Daniel S. Mount, Esq. (State Bar No. 77517)
Kathryn G. Spelman (State Bar No. 154512)
Dan Fingerman (State Bar No. 229683)
Kevin Pasquinelli (State Bar No. 246985)
Mount & Stoelker, P.C.
333 West San Carlos
RiverPark Tower, Suite 1650
San Jose CA 95110-2740
Phone: (408) 279-7000
Fax: (408) 998-1473

Attorneys for Defendants Romi Omar Mayder, Wesley Mayder, Silicon Test Systems, Inc., and Silicon Test Solutions, LLC.

MOUNT & STOELKER, P.C.
RIVERPARK TOWER, SUITE 1650
333 WEST SAN CARLOS
SAN JOSE, CALIFORNIA 95110-2711
TELEPHONE (408) 279-7000

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VERIGY US, INC, a Delaware Corporation Plaintiff, vs. ROMI OMAR MAYDER, an individual, WESLEY MAYDER, an individual, SILICON TEST SYSTEMS, INC. a California Corporation, SILICON TEST SOLUTIONS, LLC, a California Limited Liability Corporation, inclusive, Defendants.	**Civil Case No.: C07-04330 RMW (HRL)** **DECLARATION OF KEVIN M. PASQUINELLI IN SUPPORT OF DEFENDANTS RESPONSE FOR ORDER TO SHOW CAUSE RE PRELIMINARY INJUNCTION** Date: November 9, 2007 Time: 9:00 Dept.: Judge: Hon. Judge Whyte

HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

DOCUMENT SUBMITTED UNDER SEAL

Redacted for public filing

I, Kevin M. Pasquinelli, declare as follows:

1. I am an attorney with the law firm of Mount & Stoelker, P.C., counsel for Defendants Romi Omar Mayder, Wesley Mayder, Silicon Test Systems, Inc., and Silicon Test Solutions, LLC. I have personal knowledge of the facts set forth in this declaration and, if called upon to testify in this Court as to those facts, my testimony would be as stated herein.

2. Attached hereto as Exhibit A is a true and accurate copy of U.S. Patent No. 6,366,112.

3. Attached hereto as Exhibit B is a true and accurate copy of the article, "Specifications Guideline, Agilent Technologies, (2000–2001)," that was accessed on October 10, 2007 at http://metrologyforum.tm.agilent.com/spec-guide.shtml.

4. Attached hereto as Exhibit C is a true and accurate copy of Probelogic's probe card specifications.

5. Attached hereto as Exhibit D is a true and accurate copy of Wikipedia's tutorial on switches.

6. Attached hereto as Exhibit E is a true and accurate copy of the documents that were produced as VER01199–1201 (Verigy's internal financial forecasts).

7. Attached hereto as Exhibit F is a true and accurate copy of the documents that were produced as VER00980–81 [redacted] Project Datasheet dated May 24, 2006).

8. Attached hereto as Exhibit G is a true and accurate copy of the documents that were produced as VER00510–17 (Agilent's June 6, 2006 meeting slides).

9. Attached hereto as Exhibit H is a true and accurate copy of the documents that were produced as VER01199–1201 (Verigy internal memorandum analyzing Agilent's return on investment for [redacted]

10. Attached hereto as Exhibit I is a true and accurate copy of the document that was produced as VER02491 (non-confidential written correspondence disclosing the codename [redacted]).

MOUNT & STOELKER, P.C.
RIVERPARK TOWER, SUITE 1650
333 WEST SAN CARLOS
SAN JOSE, CALIFORNIA 95110-2711
TELEPHONE (408) 279-7000

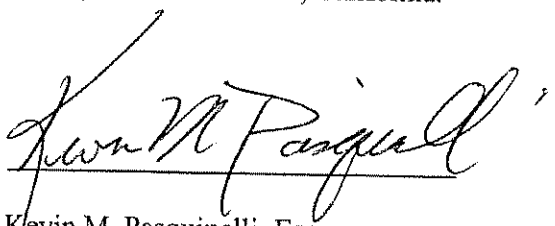
11. Attached hereto as Exhibit J is a true and accurate copy of the lead article that appeared in the September 2005 issue of *Evaluation Engineering* magazine.

12. Attached hereto as Exhibit K is a true and accurate copy of the transcript of Ira Leventhal's Deposition.

13. Attached hereto as Exhibit L is a true and accurate copy of the Honeywell HRF-SW1020 Switch Datasheet downloaded from Honeywell's website.

14. Attached hereto as Exhibit M is a true and accurate copy of transcript of Robert Pochowski's Deposition.

I declare, under penalty of perjury under the laws of the State of California, the foregoing is true and correct. Executed this 11th Day of October, 2007 in San Jose, California.



Kevin M. Pasquinelli, Esq.

MOUNT & STOELKER, P.C.
RIVERPARK TOWER, SUITE 1650
333 WEST SAN CARLOS
SAN JOSE, CALIFORNIA 95110-2711
TELEPHONE (408) 279-7000

Exhibit A

US006366112B1

(12) **United States Patent**
Doherty et al.

(10) **Patent No.: US 6,366,112 B1**
(45) **Date of Patent: *Apr. 2, 2002**

(54) **PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES**

(75) Inventors: **C. Patrick Doherty**; **Jorge L. deVarona**; **Salman Akram**, all of Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/973,509**

(22) Filed: **Oct. 9, 2001**

Related U.S. Application Data

(62) Division of application No. 09/420,256, filed on Oct. 18, 1999, now Pat. No. 6,300,786, which is a division of application No. 09/075,691, filed on May 11, 1998, now Pat. No. 6,246,250.

(51) **Int. Cl.**[7] **G01R 31/26**; G01R 31/02

(52) **U.S. Cl.** **324/765**; 324/754; 324/755; 324/757; 324/758; 324/158.1

(58) **Field of Search** 324/765, 754, 324/755, 757, 758, 158.1

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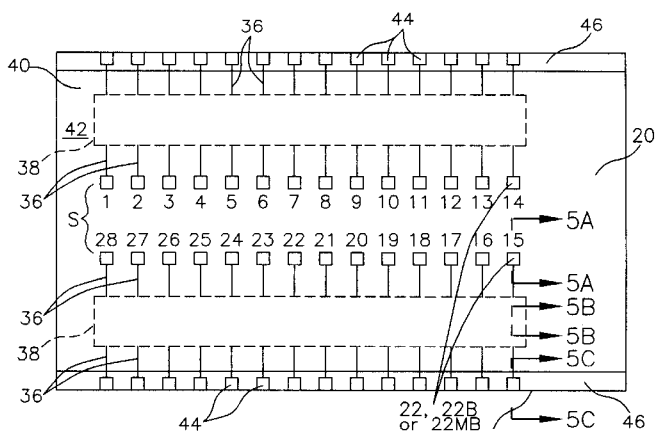
Primary Examiner—Safet Metjahic
Assistant Examiner—Wasseem H. Hamdan
(74) *Attorney, Agent, or Firm*—Stephen A. Gratton

(57) **ABSTRACT**

A probe card for testing semiconductor wafers includes probe card contacts for electrically engaging die contacts on the wafer. The probe card also includes an on board multiplex circuit adapted to fan out and selectively transmit test signals from a tester to the probe card contacts. The multiplex circuit expands tester resources by allowing test signals to be written to multiple dice in parallel. Reading of the dice can be performed in groups up to the limit of the tester resources. In addition to expanding tester resources, the multiplex circuit maintains the individuality of each die, and permits defective dice to be electrically disconnected.

21 Claims, 7 Drawing Sheets



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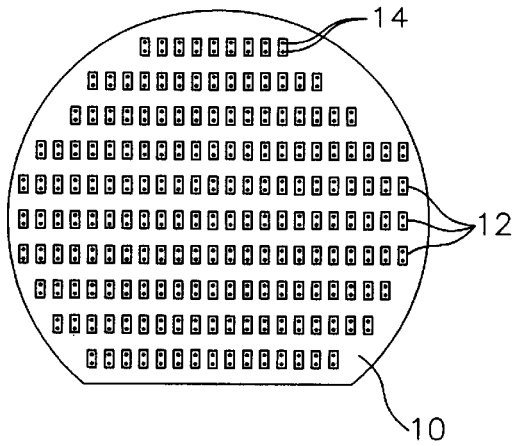

FIGURE 1
(PRIOR ART)

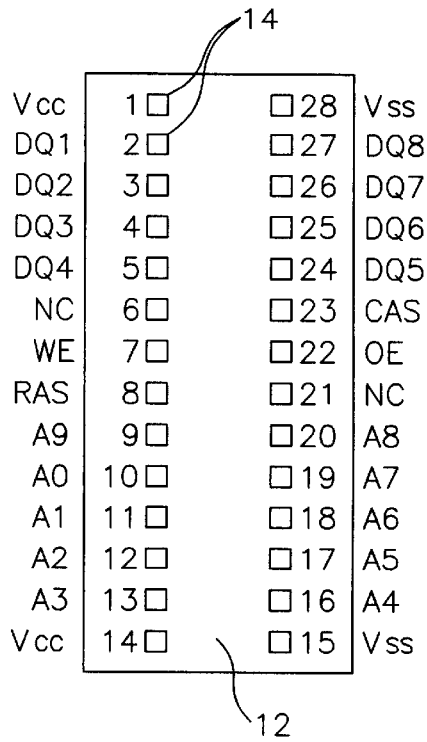

FIGURE 2
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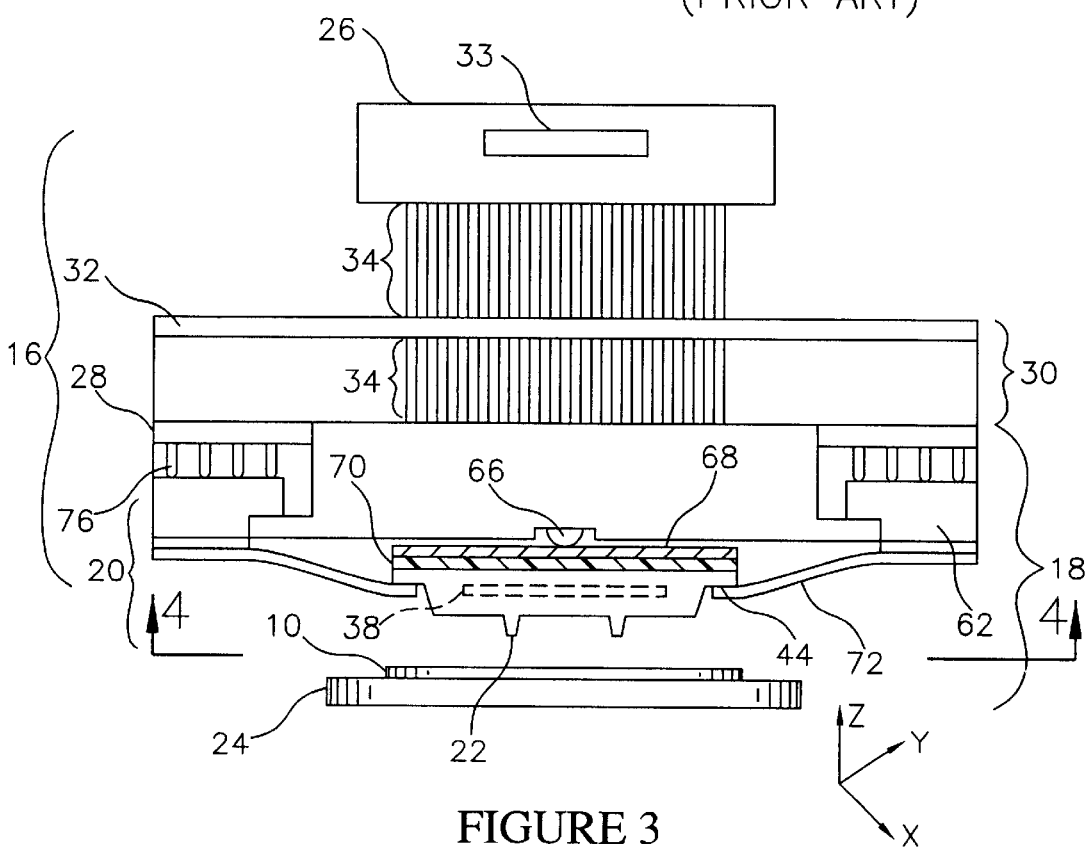

FIGURE 3

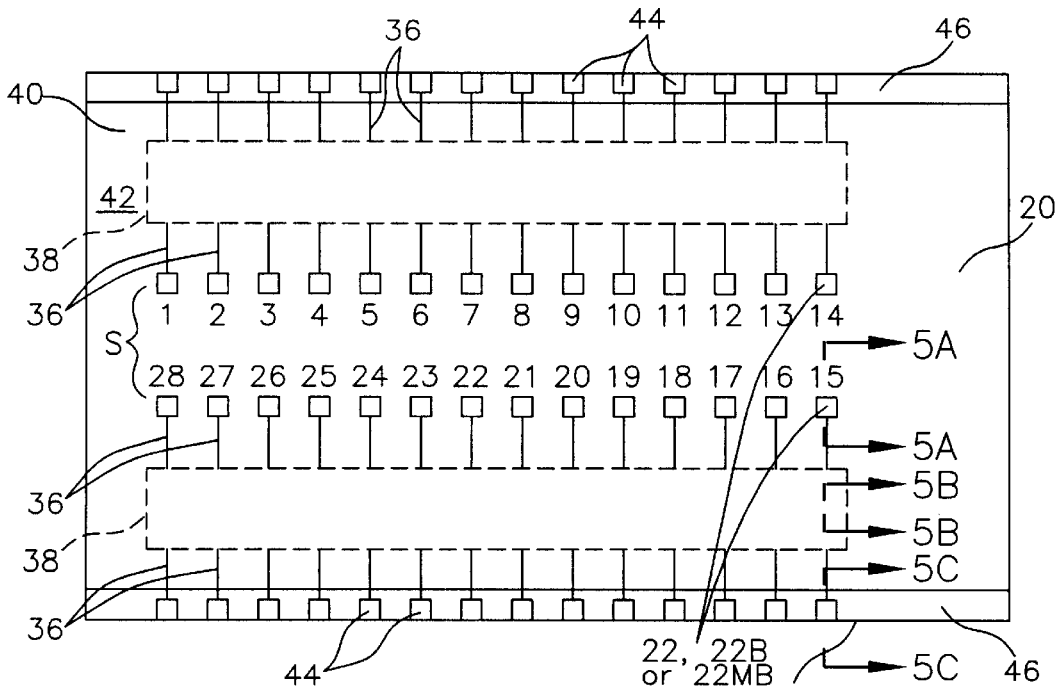

FIGURE 4

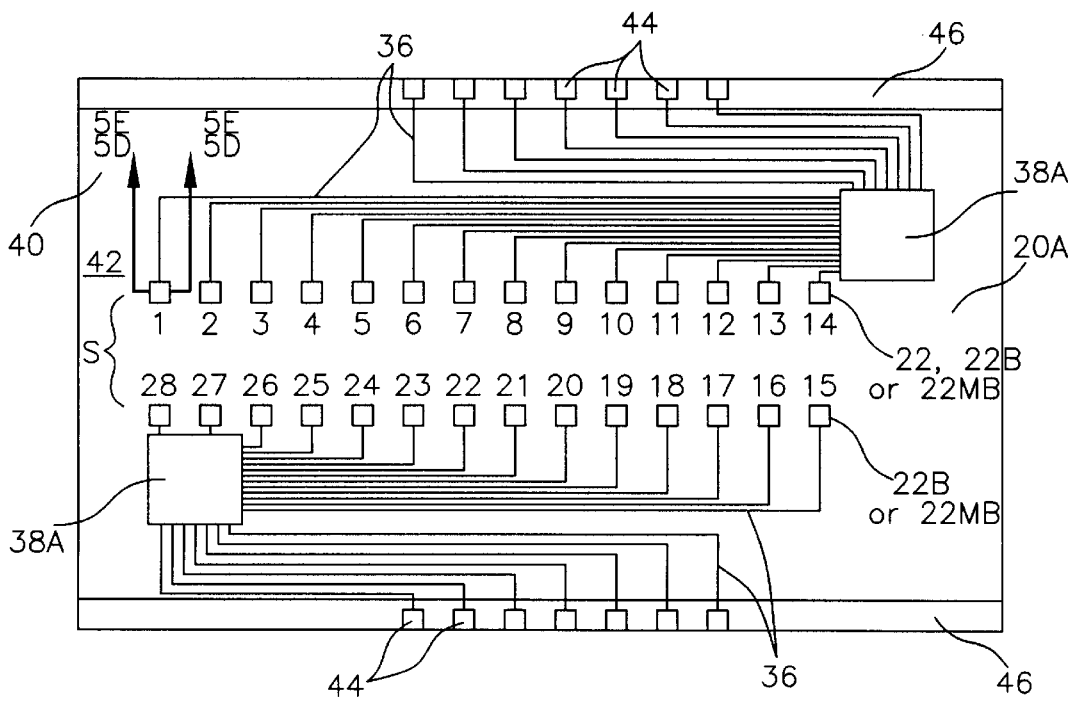

FIGURE 4A

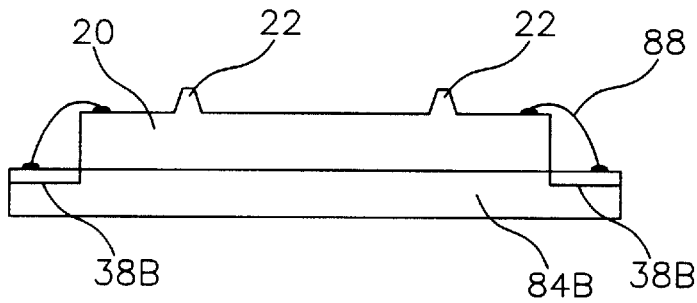

FIGURE 4B

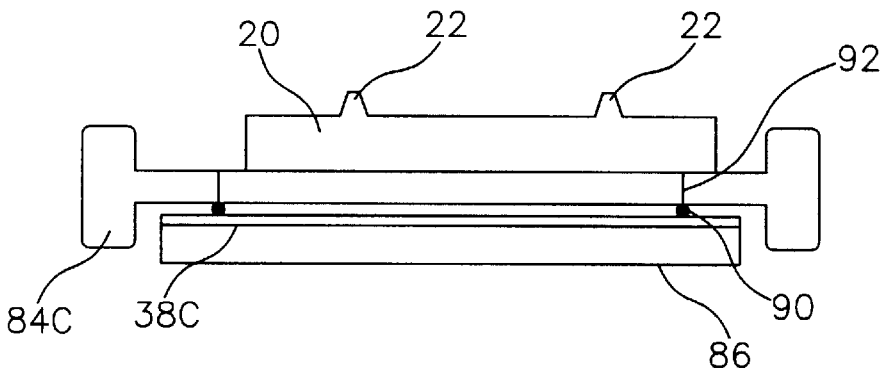

FIGURE 4C

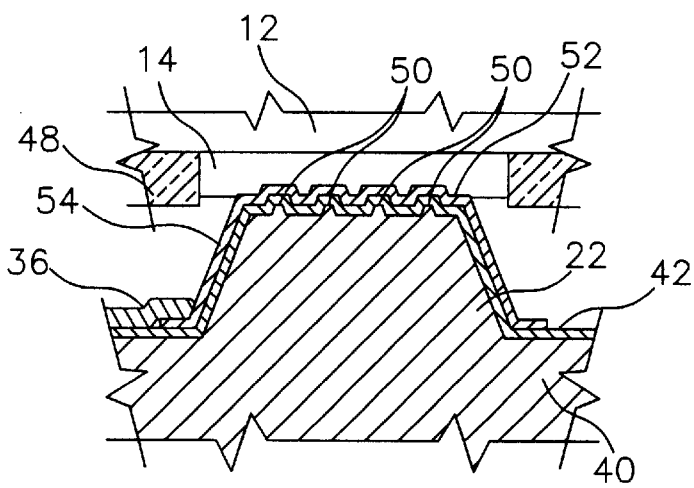

FIGURE 5A

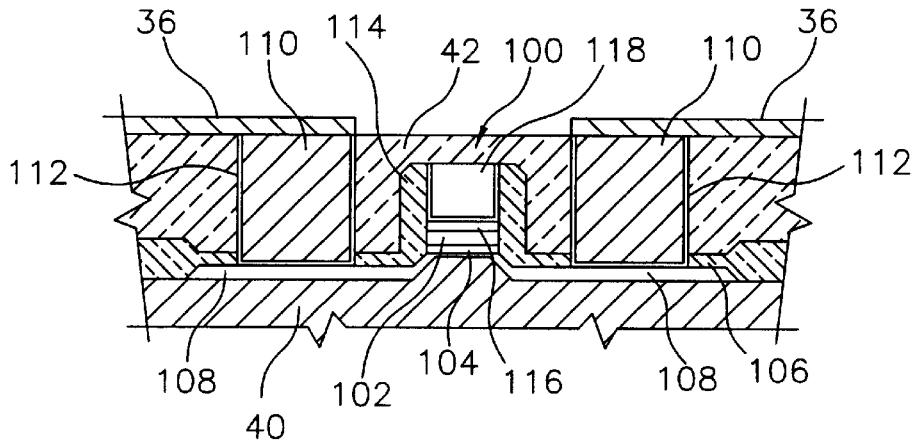

FIGURE 5B

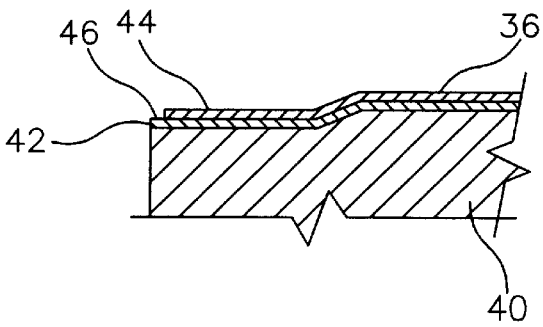

FIGURE 5C

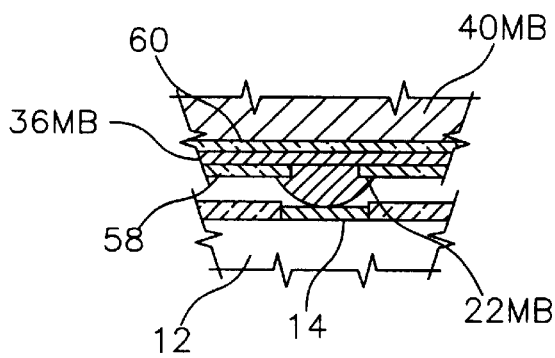

FIGURE 5D

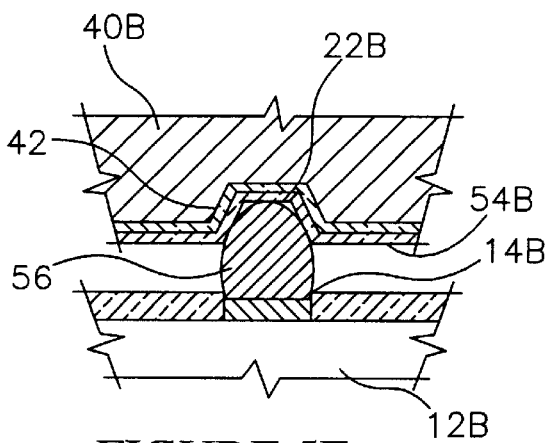

FIGURE 5E

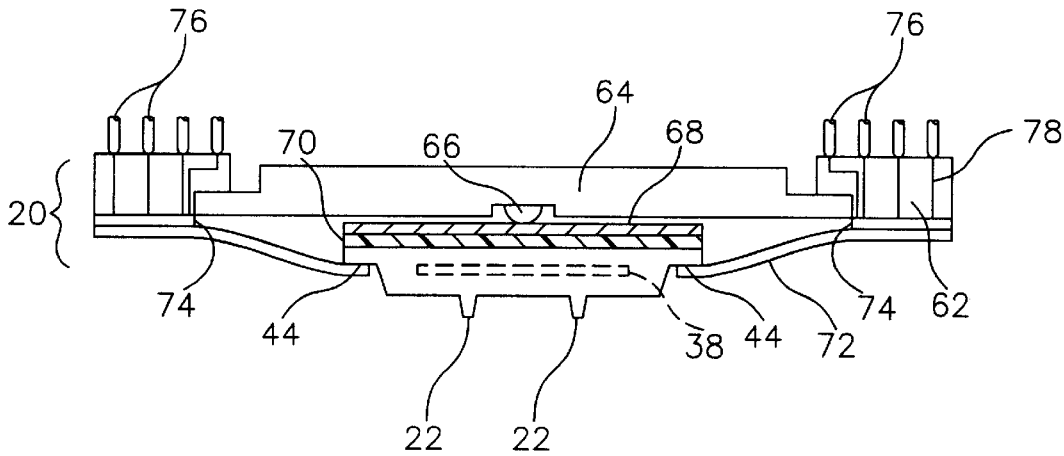

FIGURE 6

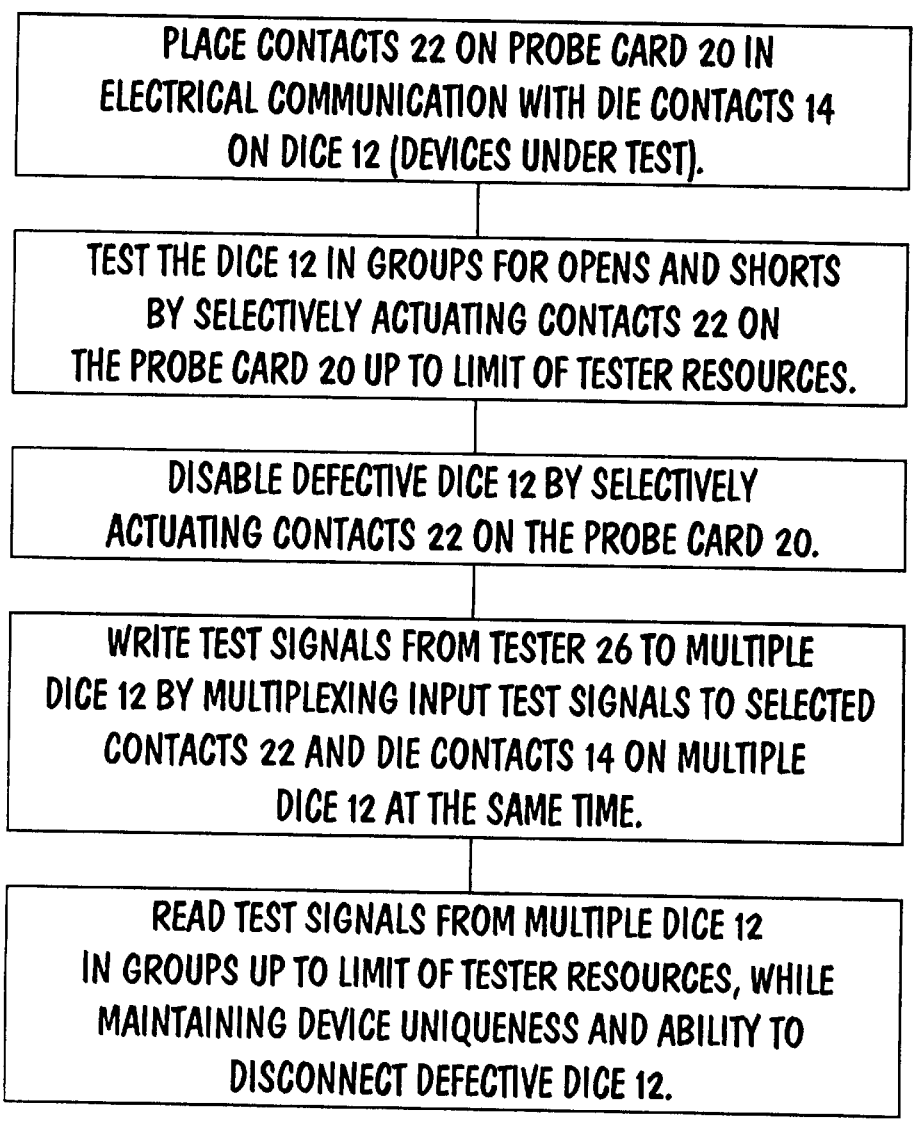

FIGURE 7

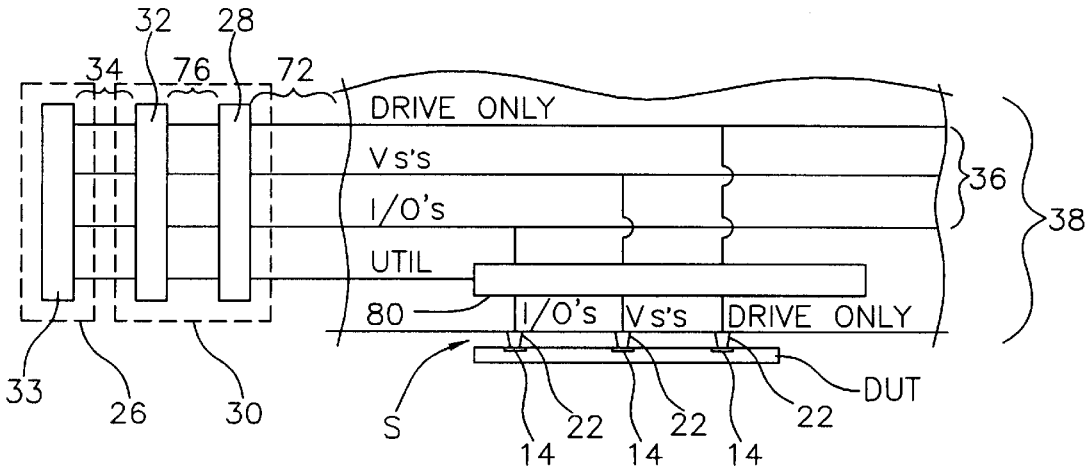

FIGURE 8A

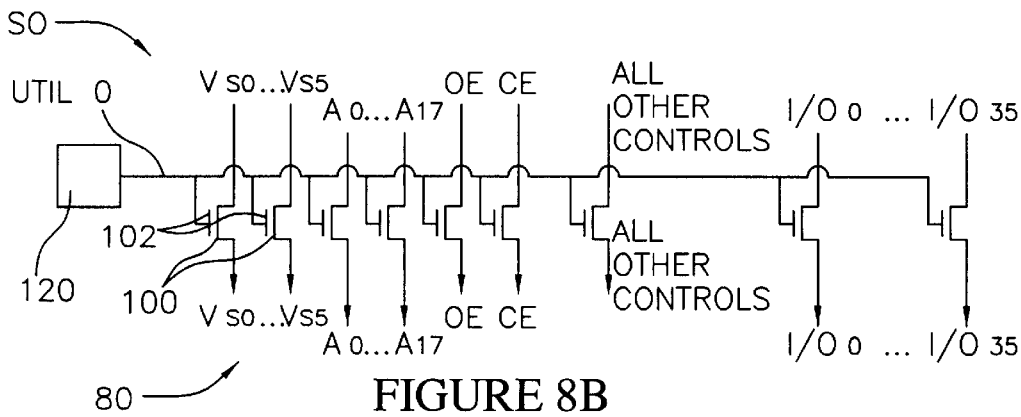

FIGURE 8B

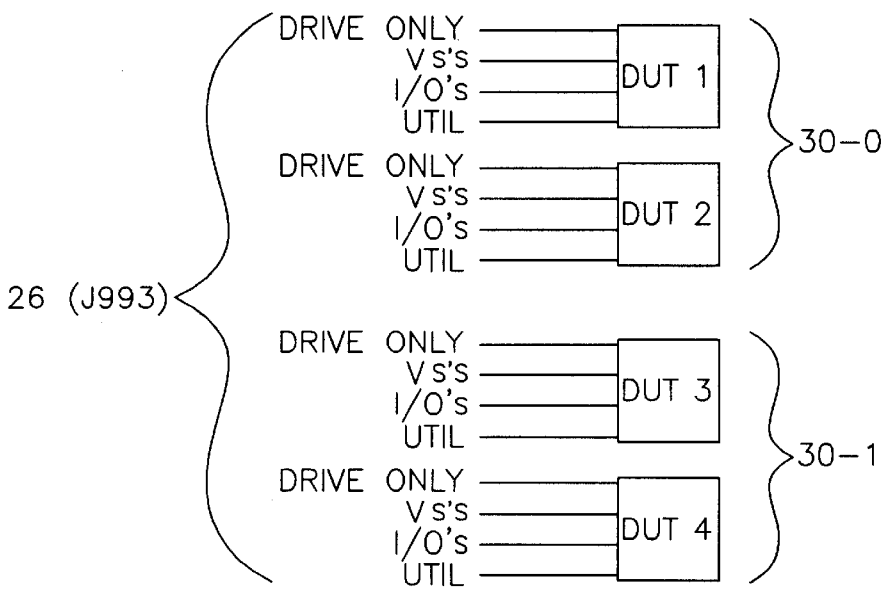

FIGURE 8C
(PRIOR ART)

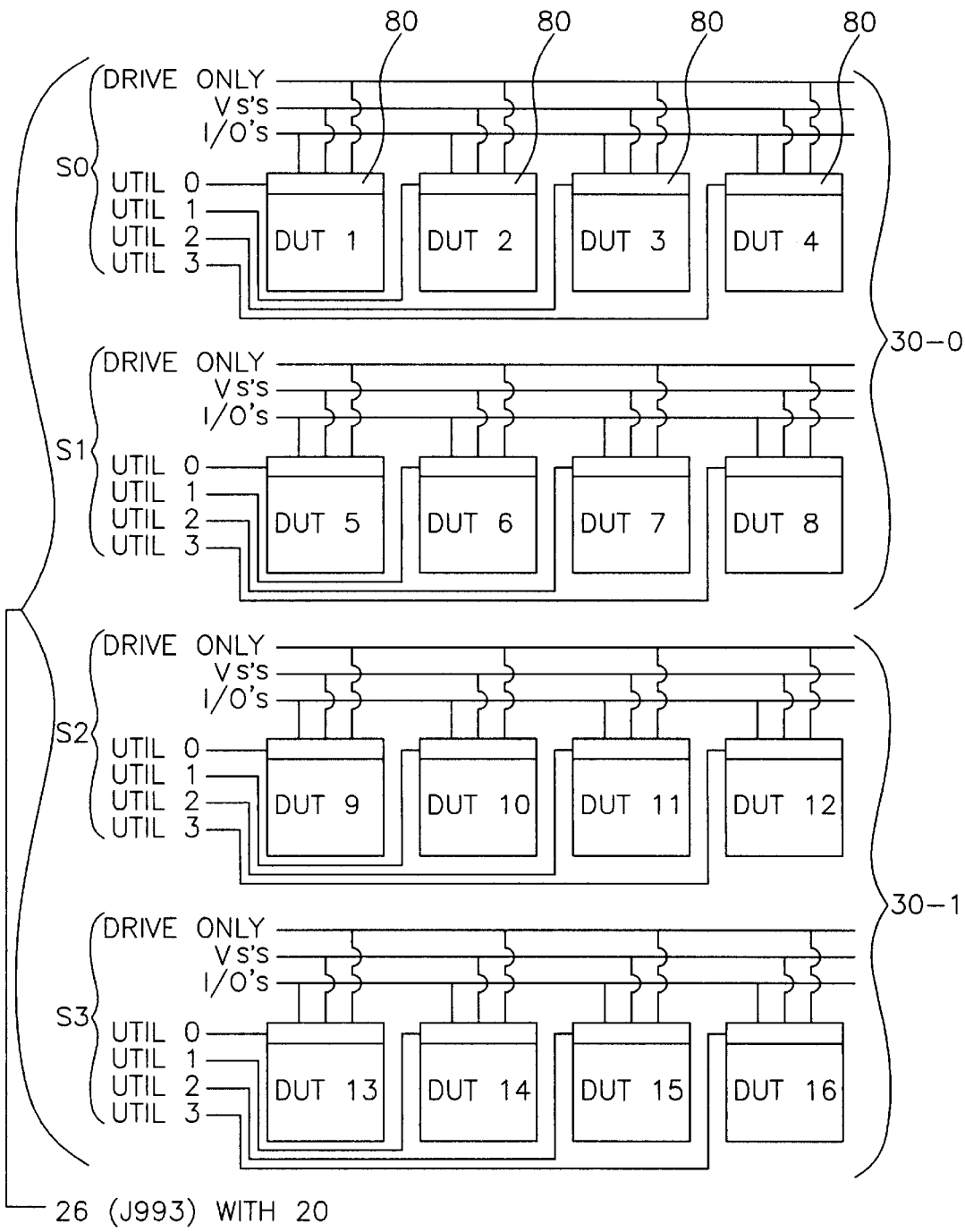
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FIGURE 8D

PROBE CARD HAVING ON-BOARD MULTIPLEX CIRCUITRY FOR EXPANDING TESTER RESOURCES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of application Ser. No. 09/420,256, filed Oct. 18, 1999, U.S. Pat. No. 6,300,786 B1, which is a division of application Ser. No. 09/075,691 filed May 11, 1998, U.S. Pat. No. 6,246,250 B1.

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture and specifically to a probe card for testing semiconductor wafers. This invention also relates to test systems and test methods employing the probe card.

BACKGROUND OF THE INVENTION

Semiconductor wafers are tested prior to singulation into individual die, to assess the electrical characteristics of the integrated circuits contained on each die. A typical wafer-level test system includes a wafer prober for handling and positioning the wafers, a tester for generating test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board to route signals from the tester pin electronics to the probe card.

The test signals can include specific combinations of voltages and currents transmitted through the pin electronics channels of the tester to the probe interface board, to the probe card, and then to one or more devices under test on the wafer. During the test procedure response signals such as voltage, current and frequency can be analyzed and compared by the tester to required values. The integrated circuits that do not meet specification can be marked or mapped in software. Following testing, defective circuits can be repaired by actuating fuses to inactivate the defective circuitry and substitute redundant circuitry.

Different types of probe cards have been developed for probe testing semiconductor wafers. The most common type of probe card includes elongated needle probes configured to electrically engage die contacts, such as bond pads, or other contacts on the wafer. An exemplary probe card having needle probes is described in U.S. Pat. No. 4,563,640 to Hasegawa et al.

Although widely used, needle probe cards are difficult to maintain and unsuitable for high parallelism applications, in which multiple dice must be tested at the same time. In addition, needle probe cards are not suitable for some applications in which the dice have high count die contact requirements, such as bond pads in dense grid arrays. In particular, the long needles and variations in the needles lengths makes it difficult to apply a constant gram force to each die contact. Long needles can also generate parasitic signals at high speeds (e.g., >500 MHZ).

A similar type of probe card includes buckle beams adapted to flex upon contact with the wafer. This type of probe card is described in U.S. Pat. No. 4,027,935 to Byrnes et al. Although better for high count die contacts, and high parallelism applications, buckle beam probe cards are expensive, and difficult to maintain.

Another type of probe card, referred to as a "membrane probe card", includes a membrane formed of a thin and flexible dielectric material such as polyimide. An exemplary membrane probe card is described in U.S. Pat. No. 4,918,383 to Huff et al. With membrane probe cards, contact bumps are formed on the membrane in electrical communication with conductive traces, typically formed of copper.

One disadvantage of membrane contact bumps is that large vertical "overdrive" forces are required to penetrate oxide layers and make a reliable electrical connection with the die contacts on the dice. These forces can damage the die contacts and the dice. In addition, membrane probe cards can be repeatedly stressed by the forces, causing the membrane to lose its resiliency. Use of high probe temperatures can also cause the membrane to lose resiliency.

Another disadvantage of membrane probe cards is the CTE (coefficient of thermal expansion) mismatch between the membrane probe card and wafer. In the future, with decreasing size of each die contact, higher parallelism requirements, and increased probing temperatures, maintaining electrical contact with the die contacts will be increasingly more difficult. In addition, because of relatively large differences between the CTE of membrane probe cards and silicon wafers, maintaining electrical contact between a large number of dice and a membrane probe card will be almost impossible.

Yet another limitation of conventional test systems, and a disadvantage of conventional probe cards, is that full functionality testing must be performed at the die level rather than at the wafer level. These tests require a large number of connections with the dice, and separate input/output paths between the dice and test circuitry. For functional test procedures on dice having multiple inputs and outputs, an input/output path must be provided to several die contacts at the same time. The number of dice that can be tested in parallel is always limited by the number of drive only, and input/output channels the tester provides, as well as the die contact arrangements on the dice. The number of drive only and input/output channels is fixed for a particular test system by its manufacturer.

To maintain speed characteristics for high count die contacts, the die contacts must be distributed throughout, or around the edges of the dice in a dense array. With this arrangement it is very difficult to parallel probe multiple dice using needle type probe cards, and impossible with dice having high count die contacts. Buckle beam probe cards are a costly alternative for probing dice having high count die contacts.

In view of the foregoing, improved probe cards capable of testing wafers with large numbers of dice, and high count die contacts, at high speeds, are needed in the art. In addition, probe cards capable of expanding tester resources to accommodate high parallelism, and high count die contact testing applications are needed in the art.

SUMMARY OF THE INVENTION

In accordance with the present invention, a probe card for testing semiconductor dice contained on a water is provided. The probe card is adapted for use with a conventional tester and wafer prober. The probe card includes an on board multiplex circuit adapted to fan out, and selectively transmit, test signals from the tester to the wafer in response to control signals. The multiplex circuit includes active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The multiplex circuit allows tester resources to be fanned out to multiple devices under test, while maintaining the uniqueness of each device, and the ability to disconnect failing devices. The additional control of the test signals also speeds up the testing process, and allows higher wafer throughputs using the same tester resources.

In addition to the multiplex circuit, the probe card includes a substrate, and a pattern of contacts formed on the substrate. During a test procedure, the probe card contacts make temporary electrical connections with die contacts on the wafer. Each probe card contact can be enabled or disabled as required by the multiplex circuit, to selectively write (send) the test signals to the die contacts, and to selectively read (receive) output signals from the die contacts.

The probe card and its contacts can be configured to electrically engage one die at a time, or multiple dice at the same time, up to all of the dice contained on the wafer. In an exemplary test procedure, dice can be tested for opens and shorts in groups corresponding to the available tester resources. Next, multiple dice can be written to in parallel by multiplexing drive only and I/O resources of the tester. Following the write step, multiple dice can be read in parallel in groups corresponding to the available tester drive only and I/O resources.

With the probe card comprising a semiconducting material such as silicon, the multiplex circuit can include integrated circuits and active electrical switching devices, formed directly on the substrate, using semiconductor circuit fabrication techniques. Alternately, the multiplex circuit can be fabricated on an interposer mounted to the probe card substrate, or on a die attached to the probe card substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view of a prior art semiconductor wafer containing multiple semiconductor dice;

FIG. **2** is a plan view of a prior art semiconductor die illustrating die contacts on a face of the die and exemplary functional designations for the die contacts;

FIG. **3** is a schematic cross sectional view of a test system constructed in accordance with the invention;

FIG. **4** is an enlarged plan view taken along section line **4**—**4** of FIG. **3** illustrating a probe card constructed in accordance with the invention;

FIG. **4**A is an enlarged plan view equivalent to FIG. **4** of an alternate embodiment probe card;

FIG. **4**B is a schematic cross sectional view of another alternate embodiment probe card;

FIG. **4**C is a schematic cross sectional view of another alternate embodiment probe card;

FIG. **5**A is an enlarged cross sectional view taken along section line **5**A—**5**A of FIG. **4**, following contact of the probe card and wafer, and illustrating probe card contacts electrically engaging die contacts on the wafer;

FIG. **5**B is an enlarged cross sectional view taken along section line **5**B—**5**B of FIG. **4**, illustrating a FET transistor of on board circuitry contained on the probe card;

FIG. **5**C is an enlarged cross sectional view taken along section line **5**C—**5**C of FIG. **4** illustrating a bonding pad on the probe card;

FIG. **5**D is an enlarged cross sectional view taken along section line **5**D—**5**D of FIG. **4**A illustrating an alternate embodiment probe card contact electrically engaging a die contact on the wafer;

FIG. **5**E is an enlarged cross sectional view taken along section line **5**E—**5**E of FIG. **4**A illustrating an alternate embodiment probe card contact electrically engaging a bumped die contact on the wafer;

FIG. **6** is an enlarged view of a portion of FIG. **3** illustrating the probe card;

FIG. **7** is a block diagram illustrating steps in a method for testing in accordance with the invention;

FIG. **8**A is a schematic electrical diagram of on board circuitry and a test site contained on the probe card and the electrical interface of the probe card and tester;

FIG. **8**B is a schematic electrical diagram of a multiplex circuit of the on board circuitry;

FIG. **8**C is a schematic electrical diagram illustrating a test operation for a tester with a prior art probe card; and

FIG. **8**D is a schematic electrical diagram illustrating a test operation for the tester of FIG. **8**C but with a probe card and multiplex circuit constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1**, a prior art semiconductor wafer includes multiple semiconductor dice **12** fabricated using processes that are well known in the art. As shown in FIG. **2**, each die **12** includes multiple die contacts **14** formed thereon. The die contacts **14** comprise metal pads in electrical communication with integrated circuits contained on the die **12**.

Following singulation of the wafer **10**, the dice **12** can be packaged. In this case, the die contacts **14** can be wire bonded to lead fingers formed on a leadframe. The singulated dice **12** can also be used in unpackaged form as known good die (KGD). In this case, the die contacts **14** can be wire bonded to a substrate, such as a printed circuit board, or alternately flip chip mounted using reflowed solder bumps. The singulated dice **12** can also be included in chip scale packages. In this case, interconnects such as conductive bumps electrically contact the die contacts **14** to establish electrical communication with external contacts on a substrate.

For illustrative purposes, each die **12** includes twenty eight die contacts **14** with the functional designations indicated in FIG. **2**. However, as is apparent, the number and functional arrangements of the die contacts **14** are merely exemplary, and other arrangements are possible.

Referring to FIG. **3**, a test system **16** constructed in accordance with the invention, and configured to test the dice **12** contained on the wafer **10**. The test system **16** includes a test head **30** and a probe card **20**. The probe card **20** includes probe card contacts **22** configured to make temporary electrical connections with the die contacts **14**. The test system **16** also includes a wafer prober **18** wherein the probe card **20** is mounted, and a tester **26** configured to apply test signals through the probe card **20**, to the dice **12** contained on the wafer **10**, and to analyze the resultant signals. The wafer prober **18** includes a probe card holder **62** for mounting and electrically interfacing with the probe card **20**. Further details of the mounting of the probe card **20** to the test head **30** will be hereinafter described.

The wafer prober **18** includes a wafer chuck **24** configured to move in X and Y directions to align the wafer **10** with the probe card **20**, and in the Z direction to move the wafer **10** into contact with the probe card **20**. One suitable wafer prober **18** is manufactured by Electroglass and is designated a Model 4080.

The test system **16** also includes a prober interface board **28** for routing test signals from the test head **30** to the probe card **20**. In addition, the prober interface board **28** can be in electrical communication with tester pin electronics **32** in the test head **30**. The tester pin electronics **32** provide separate electrical paths **34** from test circuitry **33** contained in the tester **26**, to the test head **30** and to the prober interface board **28**.

The signal generating and analyzing capability of the test circuitry **33**, and the number of separate electrical paths **34** provided by the tester pin electronics **32**, are termed herein as "tester resources". In general, the configurations of the test circuitry **33**, and of the electrical paths **34**, are fixed for a particular tester **26** by the manufacturer. For example, the test circuitry **33** can be configured to route drive only signals through some of the electrical paths **34**, and input/output channels through other of the electrical paths **34**, as required for testing a particular type of die **12**. Exemplary testers **26** are commercially available from Teradyne of Boston Mass., as well as other manufacturers.

Referring to FIG. **4**, further details of the probe card **20** are illustrated. The contacts **22** on the probe card **20** are arranged in patterns corresponding to the patterns of the die contacts **14**. Each pattern of contacts **22** represents a single test site (S). For simplicity, only one pattern of contacts **22** and one test site (S) on the probe card **20** is illustrated. However, in actual practice, the probe card **20** can include multiple patterns of contacts **22** forming multiple test sites (S1 . . . Sn) to accommodate testing of multiple dice **12** at the same time. The contacts **22** on the test site S are designated **1**–**28** in correspondence with the die contacts **14** (FIG. **2**).

In order to test multiple dice **12** at the same time certain conditions must be met. Firstly, the patterns of contacts **22** must exactly match the patterns of the die contacts **14**. In addition, the stepping distance (i.e., x-y repeat and pattern spacing) must be the same for the contacts **22** as for the die contacts **14**. Secondly, the software that controls the stepping process must be able to pick valid test sites. For example, when testing at the edges of a round wafer with a probe card that includes rectangular or square patterns of contacts **22**, some patterns of contacts **22** will not have an associated device under test. It is also desirable to not have contacts **22** contacting a passivation layer **48** (FIG. **5**A) on the dice **12** as this can damage the contacts **22**.

In general, the use of the probe card **20** can greatly reduce the number of steps necessary for the prober **18** to test all of the dice **12** contained on the wafer **10**. In the extreme case, rather than using stepping methods, the probe card **20** can be formed with enough patterns of contacts **22** to simultaneously contact every die contact **14** for all of the dice **12** on the wafer **10**. Test signals can then be selectively applied and electronically switched as required, to selected dice **12** on the wafer **10**. The probe card **20** can be formed with any desired number of test sites (S1 . . . Sn). In addition, the probe card **20** can be configured to test a complete semiconductor wafer **10**, or to test a portion of the dice **12** in a partial wafer, or other substrate.

Still referring to FIG. **4**, in addition to the patterns of contacts **22**, the probe card **20** includes patterns of conductors **36** in electrical communication with the contacts **22** and with on-board circuitry **38**. The contacts **22** and conductors **36** are formed on a substrate **40** of the probe card **20**.

In the embodiment illustrated in FIG. **5**A, the substrate **40** comprises silicon (or another semiconducting material such as gallium arsenide). This permits the on-board circuitry **38** to be formed as integrated circuits on the substrate **40** using semiconductor circuit fabrication techniques such as doping, CVD, photolithography, and etching. Also, with the substrate **40** comprising silicon, a coefficient of thermal expansion of the probe card **20** exactly matches that of the wafer **10**. The substrate **40** can also comprise a silicon containing material, such as silicon-on-glass, and the on board circuitry can be formed on a layer of the substrate **40**.

Preferably, the substrate **40** is thick enough to resist deflection and buckling during test procedures using the probe card **20**. In addition, an electrically insulating layer **42**, such as SiO_2, polyimide, or BPSG can be formed on the substrate **40** to provide insulation for the contacts **22** and conductors **36** from the bulk of the substrate **40**.

The conductors **36** on the substrate **40** are in electrical communication with the probe card contacts **22**, and with the on board circuitry **38**. The conductors **36** can be formed on a surface of the substrate **40** in a required pattern. In addition, the conductors **36** can include interlevel segments, such as metal vias or other interlevel electrical paths, that are in electrical communication with other components of the on-board circuitry **38**.

In addition, the conductors **36** can be placed in electrical communication with the test circuitry **33** to provide electrical paths from the test circuitry **33** (FIG. **3**) to the on-board circuitry **38**, and to the contacts **22**. Preferably, the conductors **36** comprise a highly conductive metal such as copper, aluminum, titanium, tantalum, tungsten, molybdenum or alloys of these metals. The conductors **36** can be formed as a single layer of metal, or as a multi metal stack, using a thin film metallization process (e.g., CVD, patterning, etching). Alternately, a thick film metallization process (e.g., screen printing, stenciling) can be used to form the conductors **36**.

The conductors **36** also include bonding pads **44** located along the peripheral edges of the probe card **20**. The bonding pads **44** provide bonding sites for forming separate electrical paths from the probe card holder **62** (FIG. **1**) to each of the conductors **36**. Preferably the bonding pads **44** are located on recessed surfaces **46** (FIG. **5**C) along the edges of the substrate **40** to provide clearance for TAB bonds, wire bonds, spring loaded connectors (e.g., "POGO PINS") or other electrical connections to the bonding pads **44**.

Referring to FIG. **5**A, the probe card contacts **22** are shown in an enlarged cross sectional view. In the embodiment of FIG. **5**A, the contacts **22** comprise raised members that project from a surface of the substrate **40**. The raised contacts **22** help to provide a separation distance between the probe card **20** and the wafer **10** to clear any particulate contaminants that may be present on the opposing surfaces. In addition, the contacts **22** can include penetrating projections **50** adapted to penetrate the die contacts **14** to a limited penetration depth. To limit the penetration depth, the penetrating projections **50** have a height that is less than a thickness of the die contacts **14**. For thin film aluminum die contacts **14**, this thickness will typically be less than about 1.0 μm. As also shown in FIG. **5**A, surfaces **52** at the tips of the contacts **22** provide stop planes for limiting penetration of the contacts **22** into the die contacts **14**. These stop plane surfaces **52** along with the dimensions of the penetrating projections **50** insures that the contacts **22** minimally damage the die contacts **14** during a test procedure.

The contacts **22** and penetrating projections **50** can be formed integrally with the substrate **40** using a bulk micromachining process. With such a process, an etch mask (e.g., Si_3N_4 layer) can be formed on the substrate **40** and a suitable etchant, such as KOH, can be used to etch the substrate **40** to form the contacts **22**. Solid areas of the etch mask determine the peripheral dimensions and shape of the contacts **22**. The etch rate and time of the etch process determine the etch depth and the height of the contacts **22**. Such a process permits the contacts **22**, and penetrating projections **50**, to be formed accurately, and in a dense array to accommodate testing of dense arrays of die contacts **14**.

A representative height of the contacts **22** can be from 50 μm to 100 μm. A representative width of the contacts **22** on

a side can be from 25 μm to 80 μm. A spacing of the contacts **22** matches the spacing of the die contacts **14**. A height of the penetrating projections **50** can be from about 2000 Å–5000 Å.

Still referring to FIG. **5**A, each contact **22** is covered with a conductive layer **54** in electrical communication with a conductor **36**. The conductive layers **54** for all of the contacts **22** can be formed of a metal layer deposited and patterned to cover the contacts **22**, or other selected areas of the substrate **40**. By way of example, the conductive layers **54** for the contacts **22** can comprise aluminum, copper, titanium, tungsten, tantalum, platinum, molybdenum, cobalt, nickel, gold, iridium or alloys of these metals. Some of these materials such as gold and platinum are non-reactive so that material transfer between the contacts **22** and the die contacts **14** can be minimized. The conductive layers **54** can also comprise a metal silicide or a conductive material such as doped polysilicon. Further, the conductive layers **54** can comprise a bi-metal stack including a base layer, and a non-reactive and oxidation resistant outer layer, such as gold or platinum.

The conductive layers **54** can be formed using a metallization process that includes blanket deposition (e.g., CVD), formation of a resist mask, and then etching. Preferably, the resist mask comprises a thick film resist that can be deposited to a thickness greater than a conventional resist. One suitable resist is a negative tone, thick film resist sold by Shell Chemical under the trademark "EPON RESIN SU-8".

The conductive layer **54** for each contact **22** is in electrical communication with a corresponding conductor **36** formed on the substrate **40**. The conductive layers **54** and conductors **36** can be formed at the same time using the same metallization process. Alternately, the conductors **36** can be formed of a different metal than the conductive layers **54** using separate metallization process.

A process for fabricating the contacts **22** on a silicon substrate, substantially as shown in FIG. **5**A is described in U.S. Pat. No. 5,483,741, entitled "METHOD FOR FABRICATING A SELF LIMITING SILICON BASED INTERCONNECT FOR TESTING BARE SEMICONDUCTOR DICE", and in U.S. Pat. No. 5,686,317 entitled "METHOD FOR FORMING AN INTERCONNECT HAVING A PENETRATION LIMITED CONTACT STRUCTURE FOR ESTABLISHING A TEMPORARY ELECTRICAL CONNECTION WITH A SEMICONDUCTOR DIE", both of which are incorporated herein by reference.

Referring to FIG. **5**B, an enlarged cross sectional view of a FET transistor **100** of the on board circuitry **38** is illustrated. As is apparent the FET transistor **100** is merely one component of the on board circuitry **38**. The on board circuitry **38** can include many FET transistors **100**, as well as additional components, to provide the circuit arrangements that will be hereinafter explained. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor **100** illustrated in the preferred embodiment.

The FET transistors **100** can be formed integrally with the substrate **40** using semiconductor circuit fabrication techniques. A suitable process sequence can include initially etching the contacts **22** (FIG. **5**A) and penetrating projections **50** (FIG. **5**A) and then fabricating the FET transistors **100**. Following formation of the FET transistors **100**, the insulating layer **42** can be formed, the conductive layers **54** (FIG. **5**A) can be formed, and the conductors **36** can be formed. Each FET transistor **100** includes a polysilicon gate **102**, and a gate oxide **104**. In addition, a field oxide **106** is formed on the substrate **40** for electrically isolating the FET transistors **100**. The substrate **40** also includes N+ active areas **108**, which can be formed by implanting dopants into the substrate **40** to form the sources and drains of the FET transistors **100**. Metal filled vias **110** with metal silicide layers **112**, electrically connect the sources and drains of the FET transistors **100** to the conductors **36**. The FET transistors **100** also include spacers **114**, TEOS layers **116** and nitride caps **118**.

Referring to FIG. **4**A, an alternate embodiment probe card **20**A is illustrated. The probe card **20**A is substantially similar to the probe card **20** previously described, but includes on board circuitry **38**A formed on a surface of the substrate **40** rather than being formed integrally therewith. For example, the on board circuitry **38**A can be included in a separate die mounted to the substrate **40**, and then interconnected to the conductors **36**. In this case the die containing the on board circuitry can be wire bonded or flip chip mounted to the substrate **40** in electrical communication with the contacts **14**. In this embodiment the substrate **40** can comprise silicon, ceramic, or a glass filled resin (FR-4).

As another alternative, the on board circuitry can be included on an interposer attached to the probe card **20**. Examples of interposers are shown in FIGS. **4**B and **4**C. In FIG. **4**B, an interposer **84**B includes on-board circuitry **38**B, substantially as previously described. The interposer **84**B can comprise a semiconducting material such as silicon, in which case the on-board circuitry **38**B can be fabricated on the interposer **84**B using semiconductor circuit fabrication techniques. Wire **88** can then be bonded to pads on the probe card **20** and to pads on the interposer **84**A to provide separate electrical paths there between.

Alternately, as shown in FIG. **4**C, on-board circuitry **38**C can be contained on a die **86** attached to an interposer **84**C (or directly to the probe card **20**). In the embodiment of FIG. **4**C, the die **86** is flip chip mounted to the interposer **84**C. Reflowed solder bumps **90** on the die **86** are bonded to internal conductors **92** on the interposer **84**C. In addition, the internal conductors **92** are in electrical communication with the contacts **22** on the probe card **20**.

Referring to FIG. **5**D, the probe card **20**A can include contacts **22**MB which are attached to the substrate **40** rather than being formed integrally therewith. As shown in FIG. **5**D, the probe card contacts **22**MB comprise metal microbumps formed on a polymer film **58** similar to multi layered TAB tape. In addition, conductors **36**MB are formed on an opposing side of the polymer film **58** in electrical communication with the contacts **22**MB. A compliant adhesive layer **60** attaches the polymer film **58** to a substrate **40**MB. Further details of contact **22**MB are described in U.S. Pat. No. 5,678,301, entitled "METHOD FOR FORMING AN INTERCONNECT FOR TESTING UNPACKAGED SEMICONDUCTOR DICE".

Another alternate embodiment probe card contact **22**B is illustrated in FIG. **5**E. Contacts **22**B are configured to electrically engage die contacts **14**B having solder bumps **56** formed thereon. The contacts **22**B permit a bumped die **12**B to be tested. The contacts **22**B comprise indentations formed in a substrate **40**B. In this embodiment the substrate can comprise silicon, gallium arsenide, ceramic or other substrate material. The indentations can be etched or machined to a required size and shape and then covered with conductive layers **54**B. The contacts **22**B are configured to retain the soder bumps **56**. In addition, the conductive layers **54**B for the contacts **22**B are in electrical communication with conductors equivalent to the conductors **36** previously

described. Further details of contact **22**B are described in U.S. patent application Ser. No. 08/829,193, now U.S. Pat. No. 5,962,921, entitled "INTERCONNECT HAVING RECESSED COBTACT MEMBERS WITH PENETRATING BLADES FOR TESTING SEMICONDUCTOR DICE AND PACKAGES WITH CONTACT BUMPS", incorporated herein by reference.

Referring to FIG. **6**, further details of the test system **16** and probe card **20** are illustrated. The wafer prober **18** includes the probe card holder **62**, a force applying fixture **64** and a force applying mechanism **66**. These items can be components of a conventional wafer prober as previously described. The force applying mechanism **66** presses against a pressure plate **68** and a compressible member **70** to bias the probe card **20** against the wafer **10**. By way of example, the compressible member **70** can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane **72** is bonded to the probe card **20** and to the probe card holder **62**. In general, the flexible membrane **72** functions to physically attach the probe card **20** to the probe card holder **62**. In addition, the flexible membrane **72** functions to provide electrical paths between the contacts **22** and the test circuitry **33** (FIG. **3**) of the tester **26**. The flexible membrane **72** can be formed of thin flexible materials to allow movement of the probe card **20** in Z-directions. For example, the flexible membrane **72** can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane **72** comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane **72** and corresponding conductors **74** on the probe card holder **62**. In addition, bonded connections are formed between the conductors on the membrane **72** and the bonding pads **44** on the probe card **20**.

Still referring to FIG. **6**, the wafer prober **18** includes spring loaded electrical connectors **76** which are in electrical communication with the prober interface board **28**. One type of spring loaded electrical connector **76** is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors **76** electrically communicate with internal conductors **78** on the probe card holder **62**.

The probe card mounting arrangement shown in FIG. **6**, as well as others, are described in U.S. patent application Ser. No. 08/797,719, entitled "PROBE CARD FOR SEMICONDUCTOR WAFERS AND METHOD AND SYSTEM FOR TESTING WAFERS", incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary and the probe card **20** can be mounted in a conventional manner on a commercially available wafer prober.

Test Method

Referring to FIG. **7**, steps in a method for testing the wafer **10** using the test system **18** and probe card **20** are illustrated. These steps are as follows.

1. Place contacts **22** on probe card **20** in electrical communication with die contacts **14** on dice **12** (devices under test).
2. Test the dice **12** in groups for opens and shorts by selectively actuating contacts **22** on the probe card **20** up to limit of tester resources.
3. Disable defective dice **12** by selectively actuating contacts **22** on the probe card **20**.
4. Write test signals from tester **26** to multiple dice **12** by multiplexing input test signals to selected contacts **22** and die contacts **14** on multiple dice **12** at the same time.
5. Read test signals from multiple dice **12** in groups up to limit of tester resources, while maintaining device uniqueness and ability to disconnect defective dice **12**.

Multiplex Circuit

Referring to FIGS. **8**A–**8**D, further details of the on board circuitry **38** (FIG. **4**A) are illustrated. In FIG. **8**A a single test site S is illustrated. The test site S on the probe card **20** includes a pattern of contacts **22** which are configured to electrically engage die contacts **14** on a device under test DUT. As previously described, the probe card **20** is in electrical communication with the probe card holder **62**, the tester pin electronics **32**, and the test circuitry **33** within the tester **26**.

As shown in FIG. **8**A, the on board circuitry **38** includes a multiplex circuit **80**. The multiplex circuit **80** is configured to receive test signals from the test circuitry **33** and to fan out or multiply the test signals. In addition, the multiplex circuit **80** is configured to selectively address the fanned out test signals through the probe card contacts **22** to selected die contacts **14** on the DUT. Stated differently, the multiplex circuit permits the test signals to be fanned out, allowing test procedures to be conducted in parallel. At the same time, the multiplex circuit **80** is configured to maintain the uniqueness of individual DUTs, and to electrically disconnect defective DUTs as required.

As shown in FIG. **8**A, the multiplex circuit **80** includes a Util channel for each DUT, which functions as a control channel. In addition to the Util channel, the multiplex circuit **80** includes drive only channels, Vs channels, and I/O channels. The numbers of the channels are determined by the tester resources. Table I lists the tester resources of a model "J993" tester **26** manufactured by Teradyne.

TABLE I

Tester Resources of Teradyne "J993" Tester
16 power supply channels per test head (30)
16X, 16Y address generation channels per test head (30)
16 DUTs can be tested in parallel per test head (30)
72 I/O channels per test head (30)
2 heads (30) per tester (26)
320 drive only channels per head (30) divisible as follows:
80 per test site (S) with 4 test sites (S0–S3)
40 per test site (S) with 8 test sites (S0–S7)
20 per test site (S) with 16 test sites (S0–S15)
Up to 320 megabits of catch RAM
36 Util channels per test head (30)

Table II lists the tester resources of a model "J994" tester **26** manufactured by Teradyne.

TABLE II

Tester Resources of Teradyne "J994" Tester
32 power supply channels per test head (30)
16X, 16Y address generation channels per test head (30)
32 DUTs can be tested in parallel per test head (30)
144 I/O channels per test head (30)
2 heads (30) per tester (26)
640 drive only channels per head 30 divisible as follows:
80 per test site (S) with 8 test sites (S1–S8)
40 per test site (S) with 16 test sites (S1–S16)
20 per test site (S) with 32 test sites (S1–S32)
Up to 640 megabits of catch RAM
52 Util channels per test head (30)

Table III lists the test requirements for one type of SRAM.

TABLE III

Sample SRAM Requirements For Each Device Under Test DUT
36 I/O channels per DUT
18 address channels (drive only) per DUT
32 control channels (drive only) per DUT
6 power supply channels (Vs-voltage supplies) per DUT
Util channels used depends on parallelism
Total
36 I/O channels per DUT
50 drive only channels per DUT
6 Vs channels per DUT

With these sample requirements a "J993" tester **26** can test two DUTs per test head **30**, due to the I/O requirements. This is shown schematically in FIG. **8**C. In FIG. **8**C, the (J993) tester **26** includes a first test head **30-0** and a second test head **30-1**. Each test head **30-0**, **30-1**, is capable of testing two DUTs, for a total of four at a time. Following testing of these four DUTs, both wafers **10** (one on each test head) can be stepped such that four additional DUTs align with the probe card contacts for testing.

A "J994" tester **26** has twice the tester resources of a "J993" tester **26**. Accordingly on the basis of the above sample I/O requirements, a "J994" tester **26** can test four DUTs per test head **30**, for a total of eight at a time.

Referring to FIG. **8**B, a single test site S of the multiplex circuit **80** is illustrated. The multiplex circuit **80**, simply stated, comprises multiple FET transistors **100** configured to provide a switching circuit for selectively enabling and disabling the contacts **22** on the probe card **20**. The gate **102** of each FET transistor **100** is in electrical communication with the Util **0** channel. A controller **120** (or computer) generates control signals which are transmitted through the Util **0** channel to the FET transistors **100**.

In the illustrative embodiment the multiplex circuit **80** is configured to test the SRAM of Table III. Accordingly, there are six Vs channels (Vs**0** . . . Vs**5**), eighteen address channels (A**0** . . . A**17**), and thirty six I/O channels (I/O**0**–I/O**35**). In addition, there is an OE channel, a CE channel, and an "all other controls" channel. With this arrangement test signals can be transmitted from the test circuitry **33** and latched by the channels. Control signals from the controller **120** then control the FET transistors **100** to enable and disable the contacts **22** to selectively transmit the test signals to the die contacts **14** as required.

During the test mode the uniqueness of each DUT is maintained. In addition, the control signals can be used operate the FET transistors **100** to disable selected contacts **22** in order to electrically disconnect defective DUTs. Still further, the control signals can be used to operate the FET transistors **100** to enable and disable selected contacts **22** in the transmission of "read" signals from the DUTs. However, in the "read" mode the DUTs must be read in accordance with the tester resources.

As is apparent, the multiplex circuit **80** illustrated in FIG. **8**B is merely exemplary. Those skilled in the art, with the aid of the present specification, can design other multiplex circuits able to multiply and selectively address test signals from a tester. Thus other types of multiplexing circuits are intended to be included within the scope of the present claims.

Referring to FIG. **8**D, the operation of the J993 tester **26** of Table I, outfitted with the probe card **20** having the multiplex circuit **80** is illustrated. In this example there are four test sites S**0**, S**1**, S**2**, S**4** contained in two test heads **30-0**, **30-1**. Using the multiplex circuit each test site can write test signals to four DUTs at a time. In the "read" mode the additional three DUTs per test site must be selected in accordance with tester resources (e.g., one at a time or two at a time).

A limiting factor in the number of DUTs that can be tested by each test site is the drive current capacity of the channels of the tester **26**. On the J993 and J994 testers **26**, the drive current capacity is about 50 mA per channel. In addition, the test signals can be specified with a current (IOL) of about 8 mA per channel. Thus with some margin, each I/O channel and drive only channel of the tester **26** can be configured to drive four DUTs substantially as shown in FIG. **8**D. During a write operation there is 8 mA per DUT X 4 DUTs=32 mA per tester drive only channel. This leaves a 18 mA per channel margin.

Thus the invention provides an improved probe card for testing semiconductors wafers, a method for testing semiconductor wafers using the probe card, and a test system employing the probe card. The probe card can include contacts in dense arrays to accommodate testing of multiple dice having dense arrays of die contacts. In addition, the probe card includes on board circuitry configured to expand tester resources.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts, the probe card contacts arranged in sets configured to electrically engage selected dice on the wafer;

an interposer on the substrate; and

a multiplex circuit on the interposer in electrical communication with the probe card contacts, the multiplex circuit configured to fan out test signals from a tester, and to control the probe card contacts to selectively transmit the test signals to the die contacts while the sets maintain a uniqueness of each die and disconnect defective dice.

2. The probe card of claim **1** wherein the interposer comprises a semiconductor die containing the multiplex circuit.

3. The probe card of claim **1** wherein the interposer is flip chip mounted or wire bonded to the substrate.

4. A probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts, the probe card contacts arranged in sets configured to electrically engage selected dice on the wafer;

a semiconductor die on the substrate; and

a multiplex circuit on the die in electrical communication with the probe card contacts, the multiplex circuit configured to fan out test signals from a tester, and to control the probe card contacts to selectively transmit the test signals to the die contacts, while the sets maintain a uniqueness of each die and disconnect defective dice.

5. The probe card of claim 4 wherein the die is wire bonded or flip chip mounted to the substrate.

6. The probe card of claim 4 wherein the die is mounted to an interposer attached to the substrate.

7. The probe card of claim 4 wherein the probe card contacts comprise raised members at least partially covered with conductive layers.

8. The probe card of claim 4 wherein the probe card comprises silicon and the probe card contacts comprise etched members having projections configured to penetrate the die contacts.

9. The probe card of claim 4 wherein the probe card contacts comprise microbumps on a polymer film attached to the probe card.

10. The probe card of claim 4 wherein the die contacts comprise bumps, and the probe card contacts comprise indentations configured to retain and electrically engage the bumps.

11. In a test system including a tester configured to generate test signals and having a signal writing capability, a probe card for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts comprising:

a substrate comprising a plurality of probe card contacts configured to make temporary electrical connections with the die contacts; and

a multiplex circuit on the substrate in electrical communication with the probe card contacts, the multiplex circuit configured to control the test signals to expand the signal writing capability of the tester, and to speed up the testing by multiplexing write test signals from the tester to the die contacts, by reading read test signals from selected groups of dice up to the signal reading capability, and by controlling the probe card contacts to disable defective dice.

12. The probe card of claim 11 wherein the multiplex circuit is contained on a die wire bonded or flip chip mounted to the substrate.

13. The probe card of claim 11 wherein the multiplex circuit is contained on a die mounted to an interposer attached to the substrate.

14. The probe card of claim 11 wherein the multiplex circuit is contained on an interposer attached to the substrate.

15. In a test system for testing a semiconductor wafer containing a plurality of dice having a plurality of die contacts, the system including a tester configured to generate and analyze test signals and having tester resources determined by a signal generating, transmitting and analyzing capability thereof, a probe card for applying the test signals to the dice comprising:

a substrate comprising a plurality of probe card contacts in electrical communication with the tester and configured to make temporary electrical connections with the die contacts;

a semiconductor die on the substrate; and

a multiplex circuit on the die in electrical communication with the probe card contacts, the multiplex circuit configured to control the test signals to speed up the testing, by fanning out the write test signals to multiple dice, and by reading the read test signals in groups up to a limit of the tester resources.

16. The probe card of claim 15 wherein the die is flip chip mounted or wire bonded to the substrate.

17. The probe card of claim 15 wherein the die is mounted to an interposer attached to the substrate.

18. The probe card of claim 15 wherein the multiplex circuit is contained on an interposer attached to the substrate.

19. The probe card of claim 15 wherein the probe card contacts comprise raised members at least partially covered with conductive layers.

20. The probe card of claim 15 wherein the probe card contacts comprise microbumps on a polymer film attached to the probe card.

21. The probe card of claim 15 wherein the die contacts comprise bumps, and the probe card contacts comprise indentations configured to electrically engage the bumps.

* * * * *

Exhibit B

Metrology Forum : Worldwide

Specifications Guideline

Agilent Technologies has definitions for its Test & Measurement product specifications and how they are presented. The following material is extracted from these manufacturing recommendations. Some of the practices may not apply to (Hewlett-Packard) products introduced before 1996, nor relate directly to those used in Agilent's worldwide service operations.

Product Specification Terminology

We begin by providing a basis for a common understanding of the language used at Agilent Technologies when discussing product specifications. *Figure 1* depicts the hierarchy of terms.

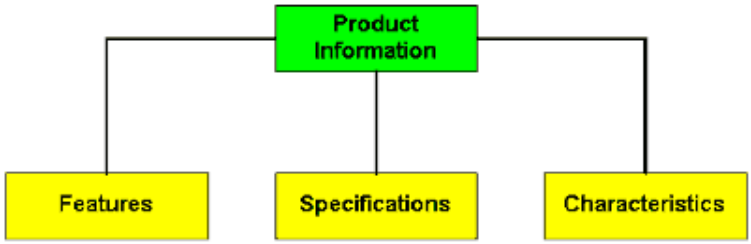

Figure 1 - Hierarchy of terms

Product information is an overall term for any attribute used to describe a product and its capabilities. It is the most general term used for discussing the property of a product.

A **feature** is an attribute of product offered as a special attraction. Features describe, or enhance, the usefulness of the product to the customer. A feature is not necessarily measurable; however, it may have an associated measurable parameter. If a feature with a measurable parameter is of interest to the customer, a product specification describes its performance. For example, HP-IB I/O interface is a feature and it is not measurable but Narrow Resolution Bandwidth Filter is a feature with the measurable parameter *bandwidth*.

Specifications formally describe product performance. A specification is a numerical value, or range of values, that bounds the performance of a product parameter. The product warranty covers the performance of parameters described by specifications. Products meet all specifications when shipped from the factory, or from an Agilent Customer Service Center following calibration.

Environmental specifications bound the external conditions applied to a product for which the specifications are valid. Some specifications are only valid over a limited, or restricted, set of external conditions but in such cases the specification includes a description of these limited conditions. The environmental specifications also define the conditions that a product may be subjected to without permanently affecting product performance or causing physical damage. These can be climatic, electromagnetic (as related to electromagnetic susceptibility), mechanical, electrical (as related to the power requirements of a product), or preconditions of operation (e.g., warm-up time or calibration interval).

Characteristics describe product performance that is useful in the application of the product, but is not covered by the product warranty. They describe performance that is typical of the majority of a given product, but is not subject to the same rigor associated with specifications.

Characteristics are often referred to as *Supplemental Characteristics*, *Typical* or *Nominal* values but these terms are not formally defined. However, *supplemental characteristic* is a generic term generally referring to all non-warranted product performance. The terms *typical* and *nominal*

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generally indicate the expected performance of a given product.

Specifications

Specifications describe the performance of parameters covered by the product warranty. The specifications do not, however, imply that any specific statistical distribution describes the performance of a parameter. Rather, the specifications simply bound the quantity of a parameter. This section outlines the model used to verify that products meet the specifications. The model was presented by Sherry Read and Timothy Read in the *Hewlett-Packard Journal* of June 1988, in their article "Statistical Issues in Setting Product Specifications".

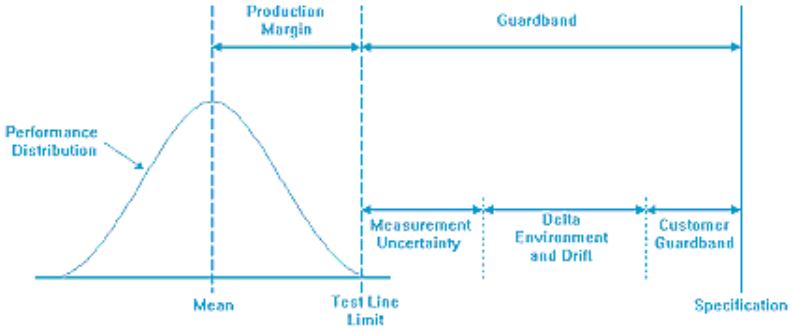

Figure 2 - Statistical model for specifications

Figure 2 depicts the statistical model for the specifications. The model represents the relationship of a measured parameter and the specification. It shows a single-sided specification but a generalization of the model represents two-sided specifications that bound both sides of a parameter. Each element of the model is described.

Guardband is the difference between the test line limit and the value of the specification. The guardband accounts for measurement uncertainties, changes in performance due to external conditions, drift and any other mechanism that may affect performance. The application of guardband ensures, with a high level of confidence, that a product measured and found to be within the test line limit will meet the specification.

The **test line limit** is the pass-or-fail limit used by the manufacturing test procedures. The manufacturing test procedures perform measurements on products but not all parameters are actually measured. The performance parameter may be inferred through statistical correlation, sample testing, or other sound means. Products found to be outside the test line limit undergo repair and re-test.

The **performance distribution** represents the unit to unit variation of a parameter measured by a manufacturing test procedure. **Production margin** is a measure of the producability of the product. The proximity of the test line limit to the performance distribution determines the size of the production margin. A small production margin results in low yields from the manufacturing test procedures. A larger production margin results in higher yields but a potentially less competitive specification.

Delta environmental represents the possible change in performance of a product over the range of external conditions applied to a product. Typically, the manufacturing test procedures execute under a limited set of external conditions; usually this is room temperature (25ºC), 10-90% relative humidity and insignificant levels of electromagnetic interference, mechanical vibration and shock. Delta environmental guardband ensures that a product tested under a limited set of conditions meets the specifications for all conditions described by the environmental specifications.

Drift represents the possible change in performance of a characteristic over the calibration interval of a product.

Typically, delta environmental and drift is determined from empirical data gathered during the characterization phase of product development. In some cases, delta environmental and drift may be theoretically derived based on relevant data from components or materials used in a product.

Measurement uncertainty represents the possible errors associated with the equipment and

the measurement techniques used during the testing of a product.

Customer guardband represents any additional guardband considered necessary to ensure that a product meets the specifications. In the majority of cases, the customer guardband is zero.

Characteristics and Supporting Specifications

Characteristics describe product performance that is useful in the application of the product, but is not covered by the product warranty. Characteristic information is representative of the product and in many cases, it may be supplemental to a specification. Characteristics are less structured than specifications. In most cases, they do not include the guardbands that are part of the specifications. Typically, determination of characteristics occurs during product development and they are not necessarily verified on all units produced.

They represent any one of the following:

- The average or median value of a parameter based on measurements from a significant number of units.
- A tolerance interval or proportion of a performance distribution derived from the measurement of a significant number of units. The proportion is typically greater than 80%.
- A parameter with a quantity that is not subject to variation (e.g., Marker Resolution). It may be either non-measurable, verifiable only through (non-traceable) functional pass-fail tests, or not be routinely measured. Nonetheless, if the feature associated with this characteristic is non-operational (and so yielding unexpected performance), the product warranty covers the repair of the failure.
- The quantity of a parameter that is not of significant importance to the customer (e.g., Product *weight*).
- The quantity of a parameter covered by a specification, but over a narrower range of conditions. For example, a specification describes the performance of a parameter over the 0 to 50ºC temperature range. A characteristic may describe the same parameter but over the 20 to 30ºC temperature range.

Supporting Specifications

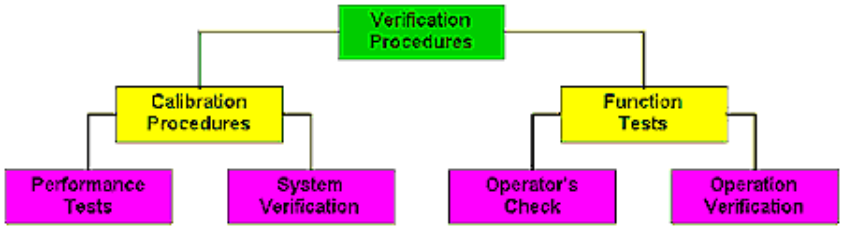

Figure 3 -- The testing hierarchy

Verification procedures are used to confirm the operation and performance of a product and include calibration procedures and function tests, as shown in *Figure 3*. Calibration procedures verify products meet specifications; function tests check them to be operational but do not necessarily verify products meet all specifications. The user documentation shipped with a product from the factory includes the verification procedures and clearly differentiate calibration procedures from function tests.

Function tests are quick tests designed to verify basic operation of a product. Function tests include operator's checks and operation verification procedures. An operator's check is normally a fast test used to verify basic operation of a product. An operation verification procedure verifies some, but not all, specifications, and often at a lower confidence level than a calibration procedure.

An **operator's check** performs a basic functional test of a product, use minimal test equipment and are run on a regular basis by the user of the product. Its purpose is to detect broken instruments; it does not verify performance to specifications. An operator's checks may be internal to a product; the procedure is executed by the product and may not require any external equipment or standards.

Operational verification (Op-Ver) tests are typically subsets of the performance tests. The purpose of operational verification tests is to verify instrument operation quickly with reasonable

confidence. Operation verification procedures typically execute faster than calibration procedures because fewer points may be tested or a test system that is less accurate than the test system used for calibration procedures is used. They are usually performed after a repair or by customers as an incoming inspection. Normally, operation verification procedures test only the major parameters covered by specifications. Operation verification procedures do not verify that a product meets all specifications.

Calibration procedures verify that products or systems operate within the specifications. *Calibration* refers to the process of measuring parameters and referencing the measurement to a calibration standard, rather than the process of adjusting products for optimum performance. Parameters covered by specifications have a corresponding calibration procedure although some parameters may only be verified at the factory because special equipment is required. Calibration procedures include both performance tests and system verification procedures, are traceable to national standards and specify adequate calibration standards.

Calibration procedures verify products meet the specifications by comparing measured parameters against a pass-fail limit which is the specification less any required guardband. The measurement uncertainty is not included as part of the guardband. Rather, the measurement uncertainty is reported along with the measured value on the test record card. Measured values that differ from the pass-fail limit by an amount less than the measurement uncertainty are specifically noted.

Calibration procedures also:

- include instructions for the operation of the standards or accessory equipment
- document the measurement uncertainty associated with each measured data point, or range of measured data points
- specify the environmental conditions
- provide a test record card
- specify any required guardbands

Operating Instructions
Calibration procedures include test method descriptions, a block diagram of the connections, and control settings for the unit-under-test and for the calibration standards. Specific setup instructions for the unit-under-test and for the standards are necessary for the operation of more complex instruments.

Environmental Specifications
The external conditions applied during the performance of the calibration procedure are specified.

Test Record Card
A test record card is prepared as a result of performing a calibration procedure. This card provides:

- reference to the test step
- a description of the measurement
- the pass-fail limits
- a space to record the actual reading
- the measurement uncertainty

Performance Tests and System Verification Procedures
Performance tests are the procedures used to verify that an instrument meets its specifications. System verification procedures are the procedures to verify a system meets its system level specifications; however, system verification procedures do not verify the individual instruments of a system.

Measurement Integrity
The technique developed to measure a particular parameter is designed to ensure that the results are traceable to standards that are external to the unit-under-test.

Exhibit C

G-Probe™ – Epoxy RF Probe Card Product Specification

Many of today's devices are mixed signal requiring a High Frequency or High Data Rate Probing Solution that is reliable, fast to design/build, and cost effective. For those customers requiring such a Probe Card, ProbeLogic designed the G-Probe™ as a simple and cost effective solution. The G-Probe™ uses Hybrid Epoxy Technology, which is a combination of standard Cantilever probes (power, ground, and low analog signals) and a special Shielded Cantilever probe for testing up to 3GHz. The result is a robust Probe Card that performs identical to standard Epoxy Probe Technology and requires no special prober setup or maintenance training.

ProbeLogic utilizes the latest State-of-the-Art Technology and Equipment to engineer, design, and manufacture high quality and "100% Tested" probe cards. ProbeLogic has the shortest turn-times and the most cost effective test solutions in the industry.

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1885 Lundy Ave.
San Jose, CA 95131
Tel: 408-416-0777
Fax: 408-943-8117
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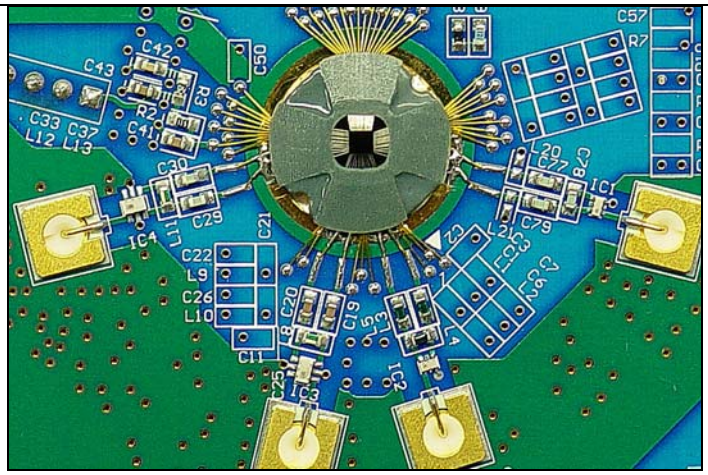


Devices

Mixed Signal/ RF	WiFi, Cell Phone, Tele Com
Pad Configuration	Single, Staggered, Dual In-line
Pad Pitch/Size (See Applications Note: 'Epoxy RF Probe Pad Guidelines')	RF Pad Pitch: ≥ 60u Standard Pad Pitch: ≥ 60u Pad Width: ≥ 55u Length: ≥ 60u
Pad Material	Gold Pads, Gold Bumps, Aluminum, Copper (or Industry Standard)
Test Frequency of Ring	Up to 3.0 GHz

Ring Assembly

Probe Ring	Custom Designed Proprietary
Probe Material	Rhenium Tungsten, Beryllium-Copper
Testing Temperature	25°C to 70°C
Probe Diameter	3.5 mils to 10 mils
Tip Diameter	0.7 mils to 5 mils
Tip Shape	Flat, Etching, or Radius
Tip Length	7 mils (or Build to Customer Spec.)
Contact Resistance	<2.0 ohms
Alignment	+/- 0.25 mils
Planarity	+/- 0.25 mils
Probe Depth	100 mils to 400 mils (Measured from bottom of PCB)
Contact Force	0.8 – 2.0 G/mils O.D.
Alignment	+/- 0.25 mils

PCB/Components

PCB Material	FR4, Polyimide, Getek, Rogers
PCB Design	Custom per Device for Maximum Performance
RF Connector	SMA, SMP, or customer specified
ATE Type	All ATE's supporting RF

Vert!™ Product Overview

M-VERT!™ Multi-DUT Vertical Probe Card Solution

M-Vert!™ Product Overview provides a brief description and general probe card specifications.

Vertical Probe Cards

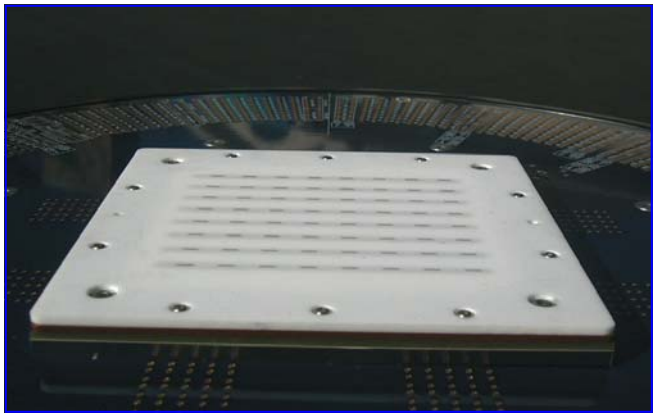
As the IC market continues to grow and die sizes continue to shrink, the test market continues to search for ways to economically test these devices. Since increasing the number of DUT's is one of the best solutions, multi-DUT vertical probe cards are becoming the choice for many test floors.

Overview

M-Vert!™ is a non-wired vertical probe card that is designed and fabricated with the customer in mind. The M-Vert!™ technology allows ProbeLogic the ability to provide a single 'turn-key' probe card solution with lower COO advantages that semiconductor test floors are requesting.

ProbeLogic has developed a unique approach to probing multi-DUT devices in configurations up to X64 DUTS. Superior probe contact and a "no-float" probe approach provides uniform contact force and electrical characteristics between the pad and the probe card.

M-Vert!™ Probe Head Designed for Efficient X64 DUT Testing



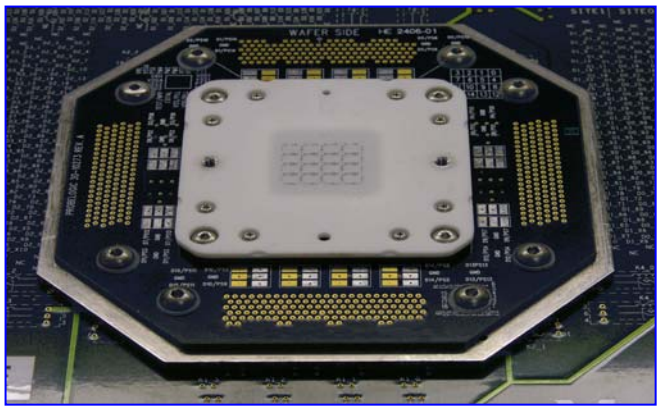
The custom designed MLO space transformer and probe head are engineered so that there is no need for exercising, fine alignment, planarity adjustments, or re-plating of the space transformer, as seen with other vertical technologies.

Space Transformer

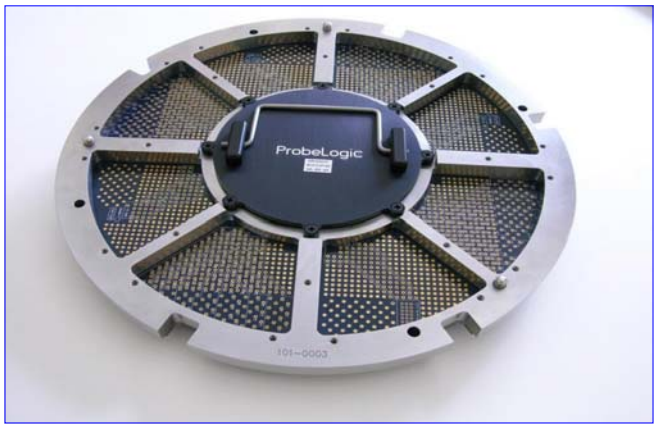
Utilizing a custom MLO Space Transformer Substrate (Interposer) that is re-flowed onto the tester PCB, a 50 ohm electrical path from tester to probe is achieved, thereby eliminating cross-talk, capacitance, and inductance issues typical of Wired Space Technology.

ProbeLogic engineers also designed the tester PCB portion to be modular and capable of reusing for a family of devices to further reduce COO.

M-Vert!™ X16 DUT Probe Head and Space Transformer Assembly



The tester side utilizes a proprietary handle assembly and cover for quick removal and probe card changeover from the test set up.



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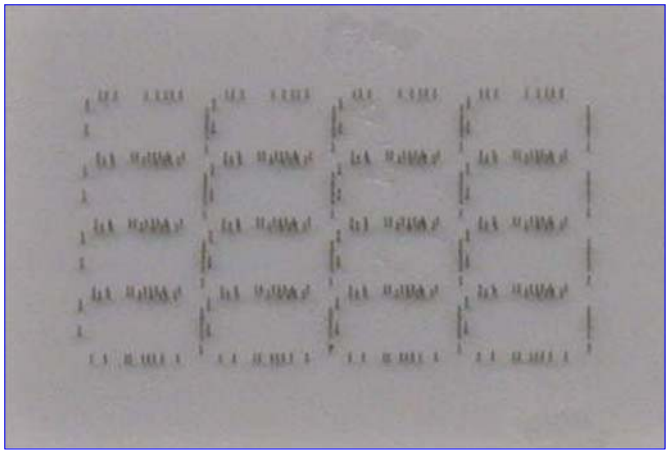
M-Vert!™ Product Overview

Manufacture and Assembly

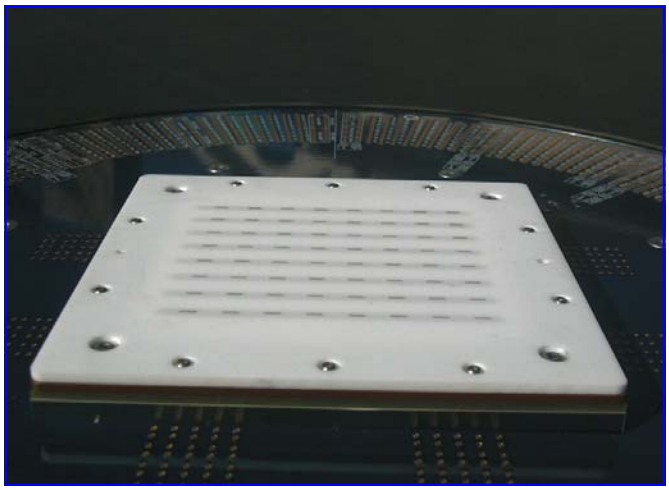
As a result of our first-rate probe contacts and strict manufacturing guidelines, M-Vert!™ is a robust solution that provides solid electrical connections and performance. Our unique assembly process maintains a tight planarity specification of +/- 1.5 mils and allows for modular probe heads. A tighter planarity specification of +/- 1.0 mils is available for non-modular applications. Either design produces an accurate gram force across the array, eliminating the need for excessive overdrive as seen with other vertical technologies.

M-Vert!™ Probe Contact View



In addition to maintaining a tight planarity window and a remarkably consistent gram force, our unique assembly process allows ProbeLogic to adhere to a tight alignment specification of +/- 0.5 mils, while not sacrificing electrical performance.

M-Vert!™ Probe Head View



M-Vert!™ STANDARD SPECIFICATIONS

Minimum Pitch Specifications:

Wire Diameter	Linear Pitch	Grid/Array Pitch
4 mils	135 um	180 um
3 mils	110 um	160 um

Alignment	+/- 12.5 um
Planarity	+/- 38u, or +/- 25u*
BCF (Contact Force 4 mil probe)	3.5 g/mil of OD
BCF (Contact Force 3 mil probe)	2.0 g/mil of OD

Maximum Current:

Wire Diameter	Probe Material	Current (A)
4 mils	P7	.6
4 mils	BeCu	2.0
3 mils	P7	.4
3 mils	BeCu	1.4

Probe Tip Options	Flat, Pointed or Wedge
Probe Tip Depth (min)	250 mils (3mil probe) 300 mils (4 mil probe)
Frequency	1-3 GHz**

*Planarity specifications are based on different assembly processes and create different end products. Please contact your technical sales representative to discuss the difference between matched sets and modular probe cards.

**Frequency is measured as bandwidth through the probe head. To gain a total understanding of the frequency that can be achieved, the PCB design, MLL/MLO substrate, and the entire test set up need to be taken into consideration to achieve higher test rates at the wafer level.

Note: These specifications are subject to change as the product develops. These are measurements taken and are minimums, but should not be taken as absolute since custom designs and specifications can be accommodated on a per device basis.

To see how ProbeLogic and M-Vert!™ can benefit your company, please contact your sales representative at:

ProbeLogic, Inc.
1885 Lundy Avenue #101
San Jose, CA 95131
408-416-0777
www.probelogic.com

probelogic

Cantilever 'Shelf' Probe Card Product Specification

ProbeLogic utilizes the latest State-of-the-Art Technology and Equipment to engineer, design, and manufacture high quality and "100% Tested" probe cards. ProbeLogic has the shortest turn-times and the most cost effective test solutions in the industry.

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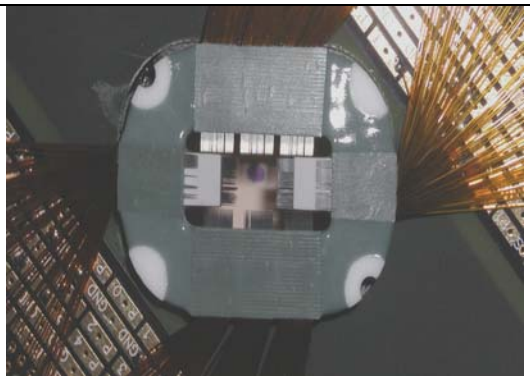


Components/Rings

Rings / Spiders	Ceramic, Aluminum, or Composite Material. (Design Per Customer Spec.)
Shelf Configurations	1x2 to 1x8 in-line; 2x2 Quad
Probe Material	Tungsten, Rhenium Tungsten, Beryllium Copper, and Palladium
Testing Temperature	25°C to 120°C
Probe Diameter	3 mils to 15 mils
Tip Diameter	0.5 mils to 10 mils
Tip Shape	Flat, Etching, or Radius
Tip Length	7 mils (or Build to Customer Spec.)
Contact Resistance	2.0 ohms
Edge Sensors	2 Wire (Left or Right Hand), 2 or 3 Wire Isolated

Devices

Device Types	Logic, Mix-Signal, Memory, LCD
Pad Configuration	Single or Staggered Row
Pad Pitch/Size	Pitch: ≥ 40 microns Width: ≥ 50 microns Length: ≥ 50 microns
Pad Material	Gold Pads, Gold Bumps, Aluminum, Copper (or Industry Standard)

Assembly

Alignment	+/- 0.2 mils
Planarity	+/- 0.2 mils
Probe Depth	80 mils to 150 mils (or Build to Customer Spec.) (Measured from tip to bottom of PCB)
Contact Force	0.8 – 3.0 G/mils O.D.
Epoxy Clearance	11 mils (Measured from tip to closest epoxy surface)
Edge Sensor Setting	*On with First Probe +/- 0.2 mils *Off with Last Probe +/- 0.2 mils
Theta Orientation	0° (+/- 0.5°)

Vert!™ Product Overview

Vert!™ - Solder Bump Vertical Probe Card Solution

Vert!™ Product Overview provides a brief description and general probe card specifications.

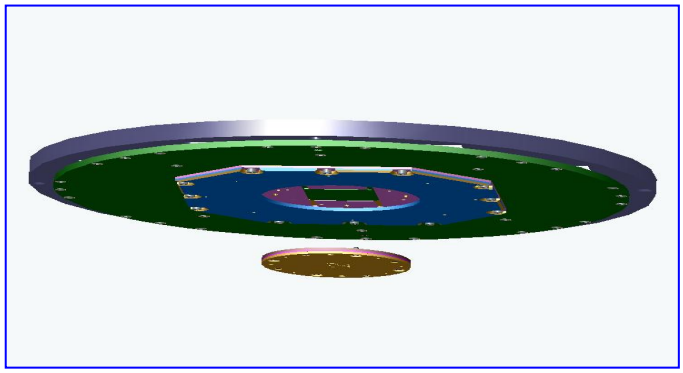
Vertical Probe Cards

As the flip chip market permeates into IC testing, technologies to probe these new devices must also evolve.

Vert!™ is a non-wired vertical probe card that is designed and fabricated with the customer in mind. The Vert!™ technology allows ProbeLogic the ability to provide a single solution with all the advantages semiconductor companies see in multiple vendors now.

Overview

ProbeLogic has developed an unique approach to probing area array solder bump devices. Superior probe contacts and a "no-float" approach provide exact contact force delivery and electrical characteristics between the bump and the probe card.



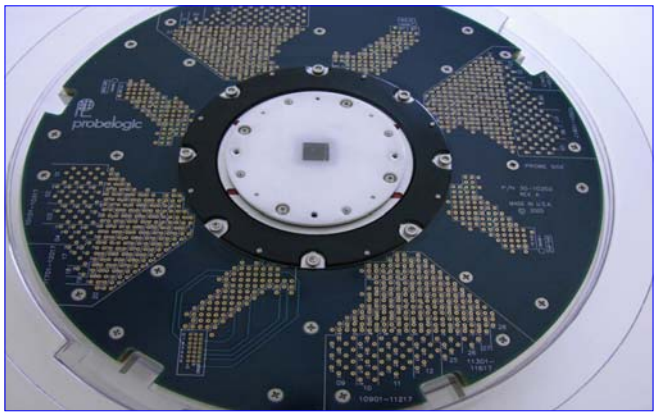
Engineering a design that is based on two components, the space transformer and probe head, Vert!™ is fast becoming the choice in vertical probe cards. ProbeLogic engineers designed these two components to be modular and swappable for any given device (refer to the ProbeLogic apps note on probe head installation and removal).

The custom designed hardware and probe head are engineered so that there is no need for exercising, fine alignment or planarity adjustments, as seen with other vertical technologies.

Space Transformer

Utilizing the customers substrate/package for the Space Transformer, the substrate is re-flowed onto the tester PCB, resulting in a 50 ohm electrical path from tester to probe, thereby eliminating cross-talk, capacitance, and inductance issues typical of Wired Space Technology.

Vert!™ Probe Head and Space Transformer Assembly



The tester side utilizes a proprietary handle assembly and cover for quick removal and probe card changeover from the test set up.

(Continued on page 2)

Vert!™ Product Overview

Manufacture and Assembly

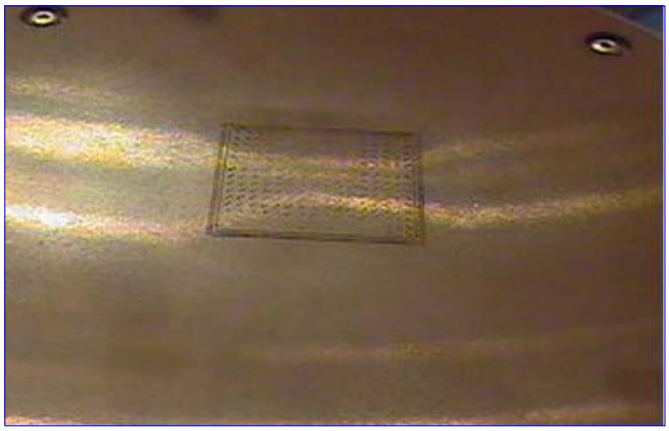
Our first-rate probe contacts and strict manufacturing guidelines prevent shorts between probes, speeds up the assembly process, and reduces customer "down time."

As a result of excellence in design, Vert!™ is a robust solution that provides solid electrical connections. Our unique assembly process maintains a tight planarity specification of +/- 1.5 mils and allows for modular probe heads. ProbeLogic can also meet a tighter planarity specification of +/- .5 mils. Either design produces an accurate gram force across the array, reducing the need for excessive overdrive as seen with other vertical technologies.

Vert!™ Probe Contact View

In addition to maintaining a tight planarity window and a remarkably consistent gram force, our unique assembly process allows ProbeLogic to adhere to a tight alignment specification of +/- 0.5 mils, while not sacrificing electrical performance.

Vert!™ Probe Head View



Vert!™ STANDARD SPECIFICATIONS**

Minimum Pitch Specifications:

Wire Diameter (mils)	Linear Pitch	Grid/Array Pitch
4	170 um	180 um
3	135 um	150 um

Alignment +/- 12.5 um
Planarity Options +/- 38u or +/- 12.5u*

BCF (Contact Force 4 mil probe) 3.5 g/mil of OD

BCF (Contact Force 3 mil probe) 2.0 g/mil of OD

Maximum Current:

Wire Diameter (mils)	Probe Material	Current (A)
4	P7	.6
4	BeCu	2.0
3	P7	.4
3	BeCu	1.4

Maximum Voltage 200 Volts

Frequency 1-3 GHz**

*Planarity specifications are based on different assembly processes and create different end products. Please contact your technical sales representative to discuss the difference between matched sets and modular probe cards.

**Frequency is measured as bandwidth through the probe head. To gain a total understanding of the frequency that can be achieved the PCB design, the customer supplied MLL, and the entire test set up need to be taken into consideration to achieve higher test rates at the wafer level.

Note: These specifications are subject to change as the product develops. These are measurements taken and are minimums, but should not be taken as absolute since custom designs and specifications can be accommodated on a per device basis.

Other helpful ProbeLogic documents:

- *MLL Space Transformer Guidelines*
- *Head Installation and Removal*
- *Vert!™ RFQ/Order Form*
- *Vert!™ Ordering Guideline*

To see how ProbeLogic and Vert!™ can benefit your company please contact your sales representative at:

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Cantilever Probe Card Specifications

Components / Rings	
Rings /Spider Material:	Ceramic, Aluminum, or Composite Materials. (Design per customer specifications)
Probe Materials:	Tungsten, Rhenium Tungsten, Beryllium Copper, NewTek, or Paliney7
Testing Temperature:	25&#65533;C to 165&#65533;C
Probe Diameter:	3 mils to 15 mils
Tip Diameter:	0.5 mils to 10 mils
Tip Shape:	Flat, Semi Radius, Full Radius
Tip Length:	7 mils (or Build to customer specifications)
Contact Resistance:	2.0 ohms
Edge Sensors:	2 Wire (Left or Right Hand), 2 or 3 wire Isolated
Devices	
Device Types:	Logic, Mixed Signal, Memory, LCD
Pad:	Single, Staggered, DRI
Pad Pitch / Size:	Pitch: $\geq$ 60u; Width: $\geq$ 55u; Length: $\geq$ 70u
Pad Material:	Gold Pads, Gold Bumps, Aluminum, Copper (or Industry Standard)
Assembly	
Alignment:	+/- 0.3 mils
Planarity:	+/- 0.3 mils
Probe Depth:	80 mils to 400 mils (or Build to Customer Spec.) (Measured from Tip to Bottom of PCB)
Contact Force:	0.8 - 3.0 G/mils O.D.
Epoxy:	11 mils (Measured from tip to closest epoxy surface)
Edge Sensor Setting:	On with First Probe +/- 0.2 mils; Off with Last Probe +/- 0.2 mils
Theta Orientation:	0&#65533; (+/- 0.5&#65533;)

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Exhibit D

Switch

From Wikipedia, the free encyclopedia

Electrical switches. Top, left to right: circuit breaker, mercury switch, wafer switch, DIP switch, surface mount switch, reed switch. Bottom, left to right: wall switch (U.S. style), miniature toggle switch, in-line switch, push-button switch, rocker switch, microswitch.

A **switch** is a device for changing the course (or flow) of a circuit. The prototypical model is a mechanical device (for example a railroad switch) which can be disconnected from one course and connected to another. The term "switch" typically refers to electrical power or electronic telecommunication circuits. In applications where multiple switching options are required (e.g., a telephone service), mechanical switches have long been replaced by electronic variants which can be intelligently controlled and automated.

The switch is referred to as a "gate" when abstracted to mathematical form. In the philosophy of logic, operational arguments are represented as logic gates. The use of electronic *gates* to function as a system of logical gates is the fundamental basis for the computer—i.e. a computer is a system of electronic switches which function as logical gates.

Contents

A simple electrical switch

A simple semiconductor switch is a transistor.

Contacts

In the simplest case, a switch has two pieces of metal called *contacts* that touch to make a circuit, and separate to break the circuit. The contact material is chosen for its resistance to corrosion, because most metals form insulating oxides that would prevent the switch from working. Contact materials are also chosen on the basis of electrical conductivity, hardness (resistance to abrasive wear), mechanical strength, low cost and low toxicity[1].

A toggle switch in the "on" position.

Sometimes the contacts are plated with noble metals. They may be designed to wipe against each other to clean off any contamination. Nonmetallic conductors, such as conductive plastic, are sometimes used.

Actuator

The moving part that applies the operating force to the contacts is called the *actuator*, and may be a **toggle** or *dolly*, a **rocker**, a **push-button** or any type of mechanical linkage *(see photo).*

Contact arrangements

A pair of contacts is said to be 'closed' when there is no space between them, allowing electricity to

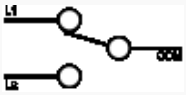
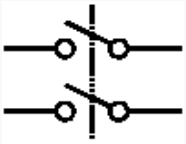
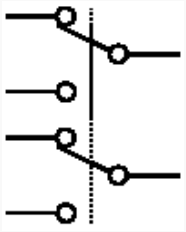
flow from one to the other. When the contacts are separated by a space, they are said to be 'open', and no electricity can flow.

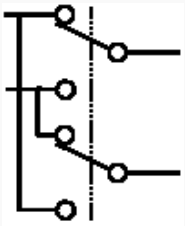
Triple Pole Single Throw (TPST or 3PST) knife switch used to short the windings of a 3 phase wind turbine for braking purposes. Here the switch is shown in the open position.

Switches can be classified according to the arrangement of their contacts. Some contacts are normally open until closed by operation of the switch, while others are normally closed and opened by the switch action. A switch with both types of contact is called a changeover switch. The simplest form of switch is the knife switch.

The terms *pole* and *throw* are used to describe switch contacts. A *pole* is a set of contacts that belong to a single circuit. A *throw* is one of two or more positions that the switch can adopt. These terms give rise to abbreviations for the types of switch which are used in the electronics industry. In mains wiring names generally involving the word *way* are used; however, these terms differ between British and American English and the terms *two way* and *three way* are used in both with different meanings.

Electronics abbreviation	Expansion of abbreviation	British mains wiring name	American mains wiring name	Description	Symbol	IEC 60617
SPST	Single pole, single throw	One way	Two way	A simple on-off switch: The two terminals are either connected together or not connected to anything. An example is a light switch.		

SPDT	Single pole, double throw	Two way	Three way	A simple changeover switch: C (Common) is connected to L1 or to L2.		
SPCO	Single pole changeover *or* Single pole, centre off			Equivalent to *SPDT*. Some suppliers use *SPCO* for switches with a stable off position in the centre and *SPDT* for those without.		
DPST	Double pole, single throw	Double pole	Double pole	Equivalent to two *SPST* switches controlled by a single mechanism		
DPDT	Double pole, double throw			Equivalent to two *SPDT* switches controlled by a single mechanism: A is connected to B and D to E, or A is connected to C and D to F.		
DPCO	Double pole changeover *or* Double pole,			Equivalent to *DPDT*. Some suppliers use *DPCO* for switches with a stable off position in the centre and *DPDT* for		

				those without.		
		Intermediate switch	4-way switch	*DPDT* switch internally wired for polarity-reversal applications: only four rather than six wires are brought outside the switch housing; with the above, B is connected to F and C to E; hence A is connected to B and D to C, or A is connected to C and D to B.		

Switches with larger numbers of poles or throws can be described by replacing the "S" or "D" with a number or in some cases the letter T (for triple). In the rest of this article the terms *SPST SPDT* and *intermediate* will be used to avoid the ambiguity in the use of the word "way".

Make-before-break, break-before-make

In a multi-throw switch, there are two possible transient behaviors as you move from one position to another. In some switch designs, the new contact is made before the old contact is broken. This is known as make-before-break, and ensures that the moving contact never sees an open circuit (also referred to as a shorting switch). The alternative is break-before-make, where the old contact is broken before the new one is made. This ensures that the two fixed contacts are never shorted to each other. Both types of design are in common use, for different applications.

Biased switches

A biased switch is one containing a spring that returns the actuator to a certain position. The "on-off" notation can be modified by placing parentheses around all positions other than the resting position. For example, an (on)-off-(on) switch can be switched on by moving the actuator in either direction away from the centre, but returns to the central off position when the actuator is released.

The momentary push-button switch is a type of biased switch. The most common type is a **push-to-make switch**, which makes contact when the button is pressed and breaks when the button is released. A **push-to-break switch**, on the other hand, breaks contact when the button is pressed and makes contact when it is released. An example of a push-to-break switch is a button used to release a door held open by an electromagnet. Changeover push button switches do exist but are even less common.

Special types

Switches can be designed to respond to any type of mechanical stimulus: for example, vibration (the *trembler switch*), tilt, air pressure, fluid level (the *float switch*), the turning of a key (*key switch*), linear or rotary movement (the *limit switch* or **microswitch**), or presence of a magnetic field (the *reed switch*).

The mercury switch consists of a drop of mercury inside a glass bulb. The two contacts pass through the glass, and are mechanically joined when the bulb is tilted to make the mercury roll on to them. The advantage of this type of switch is that the liquid metal flows around particles of dirt and debris that might otherwise prevent the contacts of a conventional switch from closing.

Other types of switch include:

- Centrifugal switch
- DIP switch
- Hall-effect switch
- Inertial switch
- Membrane switch
- Toggle switch
- Transfer switch
- Mindy switch

Intermediate switch

A DPDT switch has six connections, but since polarity reversal is a very common usage of DPDT switches, some variations of the DPDT switch are internally wired specifically for polarity reversal. They only have four

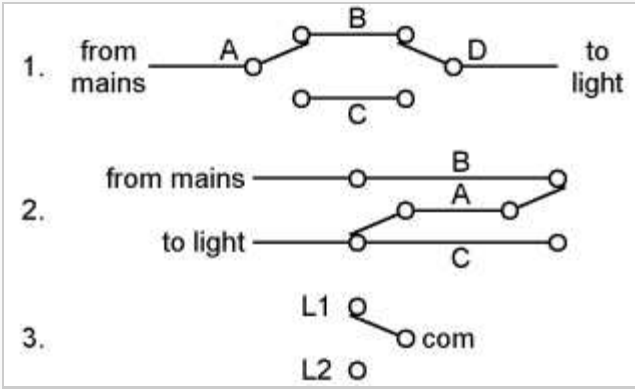
terminals rather than six. Two of the terminals are inputs and two are outputs. When connected to a battery or other DC source, the 4-way switch selects from either normal or reversed polarity. Intermediate switches are also an important part of multiway switching systems with more than two switches (see next section).

Multiway switching

Multiway switching is a method of connecting switches in groups so that any switch can be used to connect or disconnect the load. This is most commonly done with lighting.

Two locations

Switching a load on or off from two locations (for instance, turning a light on or off from either end of a flight of stairs) requires two SPDT switches. There are two basic methods of wiring to achieve this, and other not recommended.



1. First method
2. Second method
3. Labelling of switch terminals

In the first method, mains is fed into the common terminal of one of the switches; the switches are then connected through the L1 and L2 terminals (swapping the L1 and L2 terminals will just make the switches work the other way round), and finally a feed to the light is taken from the common of the second switch. A connects to B or C, D connects to B or C; the light is on if A connects to D, i.e. if A and D both connect to B or both connect to C.

The second method is to join the three terminals of one switch to the corresponding terminals on the other switch and take the incoming supply and the wire out to the light to the L1 and L2 terminals. Through one switch A connects to B or C, through the other also to B or C; the light is on if B connects to C, i.e. if A connects to B with one switch and to C with the other.

Wiring needed in addition to the mains network (not including protective earths):

First method:

- double wire between both switches
- single wire from one switch to the mains

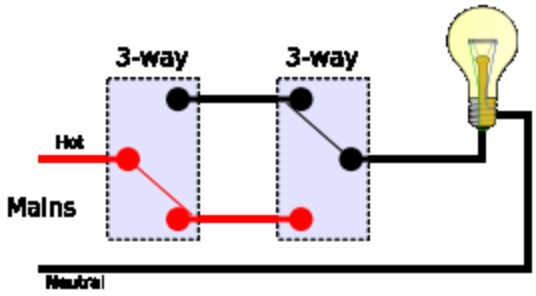
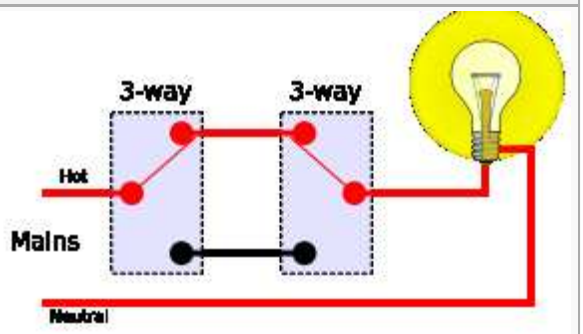
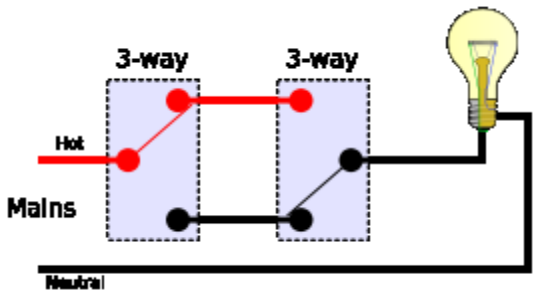
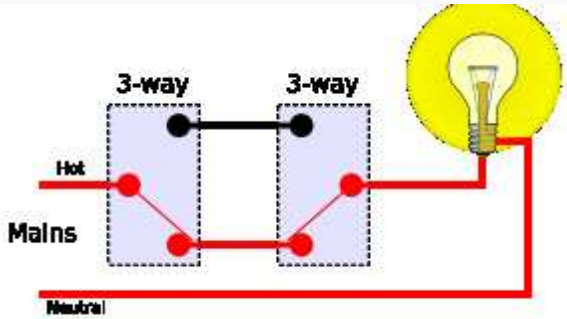
- single wire from the other switch to the load
- single wire from the load to the mains

Second method:

- triple wire between both switches
- single wire from any position between the two switches, to the mains
- single wire from any position between the two switches, to the load
- single wire from the load to the mains

If the mains and the load are connected to the system of switches at one of them, then in both methods we need three wires between the two switches. In the first method one of the three wires just has to pass through the switch, which tends to be less convenient than being connected. When multiple wires come to a terminal they can often all be put directly in the terminal. When wires need to be joined without going to a terminal a crimped joint, piece of terminal block, wirenut or similar device must be used and the bulk of this may require use of a deeper backbox.

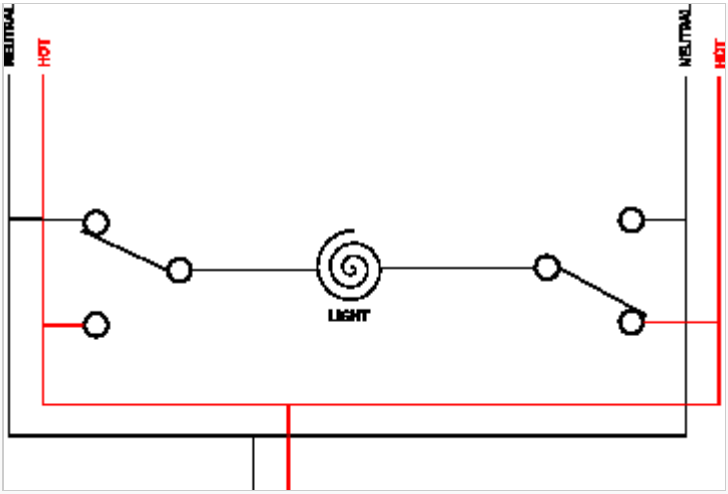
Using the first method, there are four possible combinations of switch positions: two with the light on and two with the light off.

Off	On
	
	

An unrecommended method

If there is a hot (a unique phase) and a neutral wire in both switches and just one wire

between them where the light is connected (as in the picture), you can then solve the two way switch problem easily: just plug the hot in the top from switch, the neutral in the bottom from switch and the wire that goes to the light in the middle from the switch. This in both switches. Now you have a fully functional two way switch.



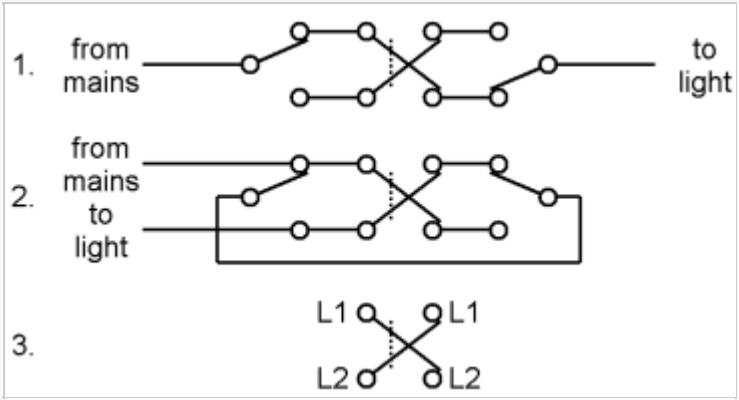
The unrecommended way using the hot and neutral directly

This works like the first method above: there are four possibilities and just in two of them there is a hot and a neutral connected in the poles of the light. In the other ones, both poles are neutral or hot and then no current flows because the potential difference is zero.

The advantage of this method is that it uses just one wire to the light, having a hot and neutral in both switches. The reason why this is not recommended is because in both switches there will be hot and neutral wires near to each other, which can lead to a short circuit more easily than in the other methods.

More than two locations

For more than two locations, the two cores connecting the L1 and L2 of the switches must be passed through an intermediate switch (as explained above) wired to swap them over. Any number of intermediate switches can be inserted, allowing for any number of locations.



Three-way switching.
1. First method
2. Second method
3. Labelling of switch terminals

Wiring needed in addition to the mains network (not including protective earths):

First method:

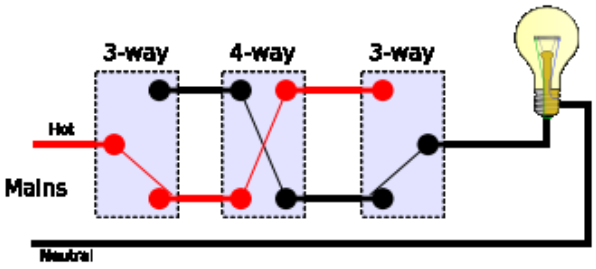
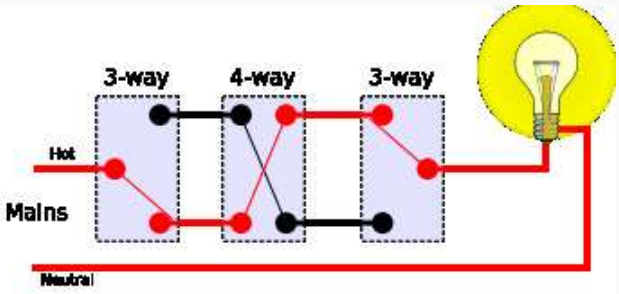
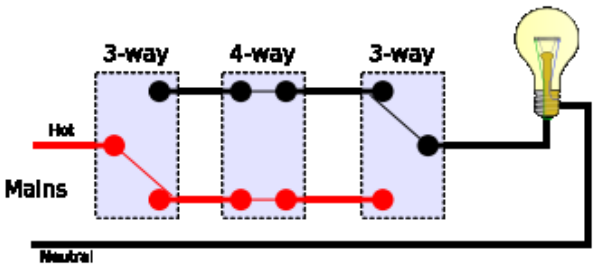
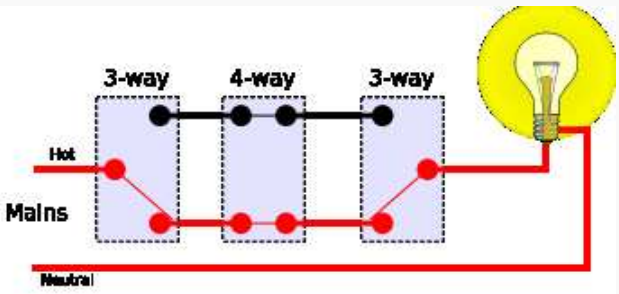
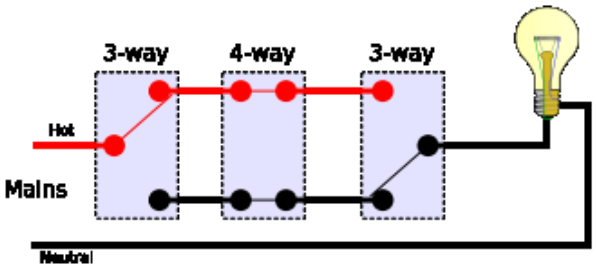
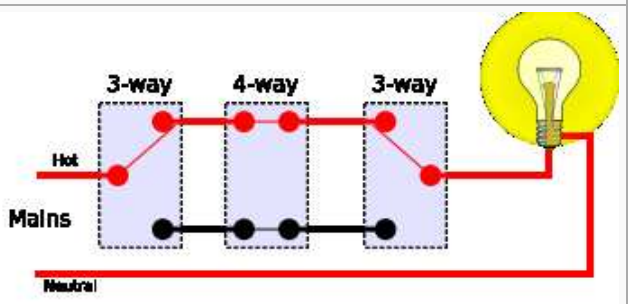
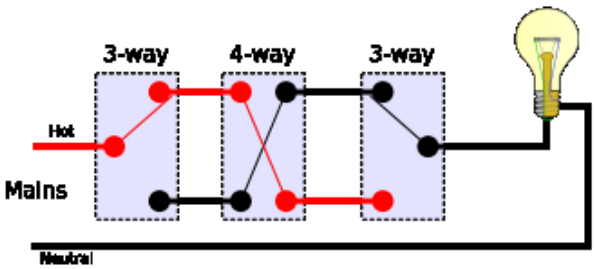
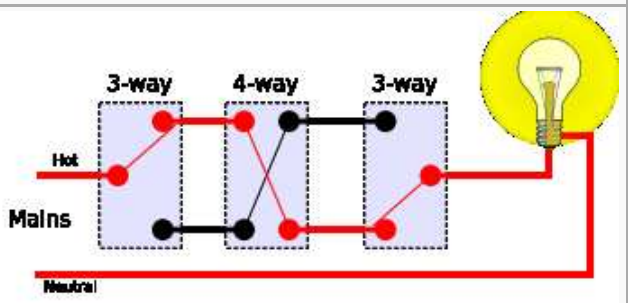
- double wire along the sequence of switches
- single wire from the first switch to mains
- single wire from the last switch to the load

- single wire (neutral) from load to mains

Second method:

- double wire along the sequence of switches
- single wire from first switch to last switch
- single wire from anywhere between two of the switches to the mains
- single wire from anywhere between the same two switches to the load
- single wire (neutral) from load to mains

Using the first method, there are eight possible combinations of switch positions: four with the light on and four with the light off.

Off	On
	
	
	
	

As mentioned above, the above circuit can be extended by using multiple 4-way switches between the 3-way switches to extend switching ability to any number of locations.

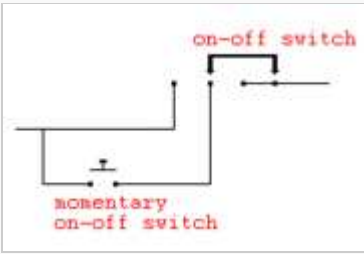
Power switching

When a switch is designed to switch significant power, the transitional state of the switch as well as the ability to stand continuous operating currents must be considered. When a switch is on its resistance is near zero and very little power is dropped in the contacts; when a switch is in the off state its resistance is extremely high and even less power is dropped in the contacts. However when the switch is flicked the resistance must pass through a state where briefly a quarter (or worse if the load is not purely resistive) of the load's rated power is dropped in the switch.

For this reason, most power switches (most light switches and almost all larger switches) have spring mechanisms in them to make sure the transition between on and off is as short as possible regardless of the speed at which the user moves the rocker.

Power switches usually come in two types. A momentary on-off switch (such as on a laser pointer) usually takes the form of a button and only closes the circuit when the button is depressed. A regular on-off switch (such as on a flashlight) has a constant on-off feature. Dual-action switches incorporate both of these features.

Contact bounce



A diagram of a dual-action switch system

Contact bounce (also called *chatter*) is a common problem with mechanical switches and relays. Switch and relay contacts are usually made of springy metals that are forced into contact by an actuator. When the contacts strike together, their momentum and elasticity act together to cause bounce. The result is a rapidly pulsed electrical current instead of a clean transition from zero to full current. The waveform is then further modified by the parasitic inductances and capacitances in the switch and wiring, resulting in a series of damped sinusoidal oscillations. This effect is usually unnoticeable in AC mains circuits, where the bounce happens too quickly to affect most equipment, but causes problems in some analogue and logic circuits that are not designed to cope with oscillating voltages.

Sequential digital logic circuits are particularly vulnerable to contact bounce. The voltage waveform produced by switch bounce usually violates

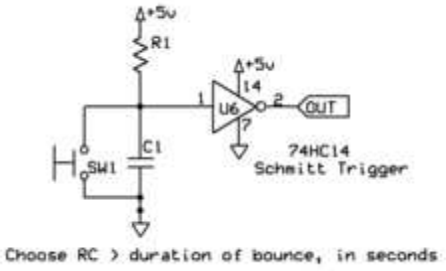
the amplitude and timing specifications of the logic circuit. The result is that the circuit may fail, due to problems such as metastability, race conditions, runt pulses and glitches.

There are a number of techniques for debouncing (mitigating the effects of switch bounce). They can be split into timing based techniques and Hysteresis based techniques.

Timing based

Timing based techniques rely on adding sufficient delays that the extra transitions introduced by bounce are ignored. Their big advantage is they do not require any special design on the switch side and so are generally cheaper. However for good performance they must be designed to suit the switch (too much delay and the response will be needlessly sluggish, too little and bounce will not be eliminated).

Resistor/Capacitor



Choose RC > duration of bounce, in seconds

If an on/off switch is used with a pull up (or pull down) resistor and a single capacitor is placed over the switch (or across the resistor, but this can cause nasty spikes of current on the power supply lines) then when the switch is closed (generally pressed) the capacitor will almost instantly discharge through the switch. But when the switch is opened (generally released) the capacitor takes some time to recharge. Therefore contact bounce will have negligible effect on the output. The slow edges can be cleaned up with a Schmitt trigger if necessary. This method has the advantage of fast response to the initial press but the current surges through the switch may be undesirable. Other RC based systems are also possible with various responses and such systems are probably the easiest method when constructing with simple logic gates and discrete components.

State machines and software

A finite state machine or software running on a CPU can be designed to wait a fixed number of clock cycles after any transition before registering another one. This provides a cheap option for debouncing when a microprocessor, microcontroller or gate array is already in use but is unlikely to be worthwhile if constructing with single logic gates.

Hysteresis

Alternatively, it is possible to build in hysteresis by making the position where a press is detected separate from that where a release is detected. As long as the bounces are small enough not to take the switch between these positions, bounce problems will be eliminated. Hysteresis can be mechanical or electronic (e.g. a Schmitt trigger).

Changeover switch

A changeover switch provides two distinct events, the making of one contact and the breaking of the other. These can be used to feed the inputs of a flip-flop. This way the press will only be detected when the pressed contact is made and the release will only be detected when the released contact is made. When the switch is bouncing around in the middle no change is detected. To get a single logic signal from such a setup a simple SR latch can be used.

Variable resistance

Normal switches are designed to give a hard on-off but it is also possible to design one that varies more gradually between the hard-on and hard-off states. This keeps the output changes caused by bouncing small. Then by feeding the output to a schmitt trigger the effect of those bounce based changes can be eliminated.

References

1. ^ General Electric Contact Materials (http://www.tanaka-precious.com/catalog/material.html) . *Electrical Contact Catalog (Material Catalog)*. Tanaka Precious Metals (2005). Retrieved on 2007-02-21.

- Walker, PMB, *Chambers Science and Technology Dictionary*, Edinburgh, 1988, ISBN 1852961503 (definition of *contact bounce*)

See also

- Circuit breaker
- Contactor
- Analogue switch
- UL, CSA, VDA
- MOSFETs

- Power symbol - the symbols commonly used on an on-off switch

External links

- Several Wiring Options (http://www.the-home-improvement-web.com/information/how-to/three-way-switch.htm) (with diagrams)
- Troubleshooting Existing 2/3/4-way Switching (http://www.thecircuitdetective.com/3and4wyinfo.htm) (US/Canada, with diagrams)
- How to Install a Three-Way Switch Short Video (http://www.milwaukeehomeinspectors.com/how-to-install-a-three-way-switch-video) (with step by step instructions)
- Tutorial about switch de-bouncing (http://www.ikalogic.com/debouncing.php) Analog and digital debouncing are discussed with schematics and example source codes

Retrieved from "http://en.wikipedia.org/wiki/Switch"

Categories: Switches | Electrical components

Exhibit E

Filed Under Seal

Exhibit F

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Exhibit G

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Exhibit H

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Exhibit I

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Exhibit J

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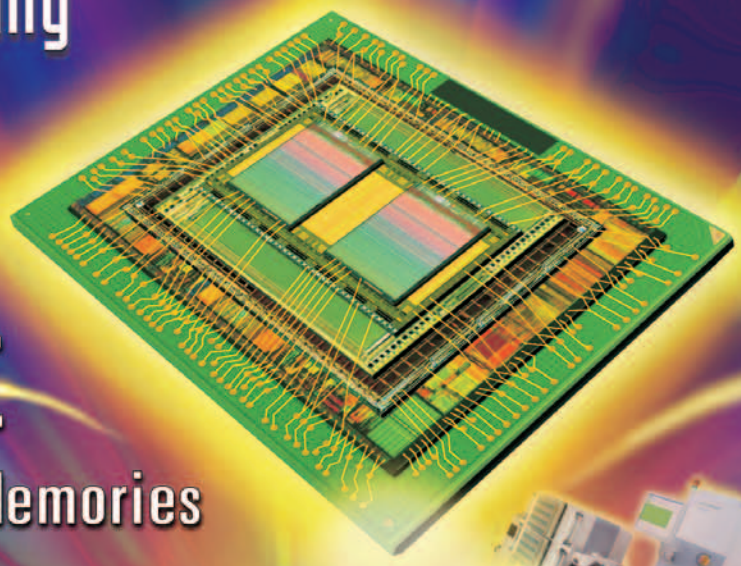
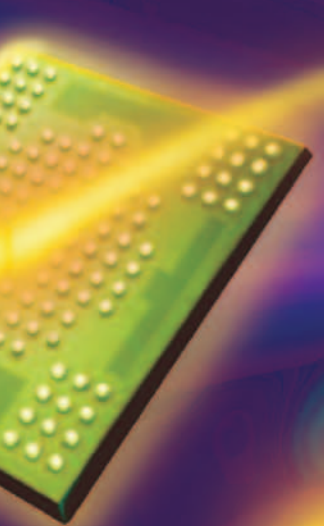
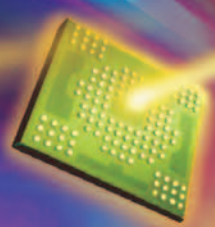
The Magazine of Electronic Evaluation and Test

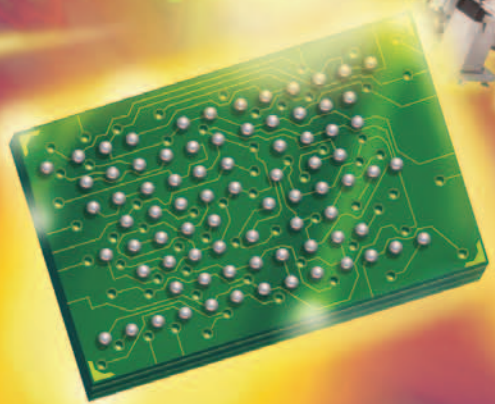


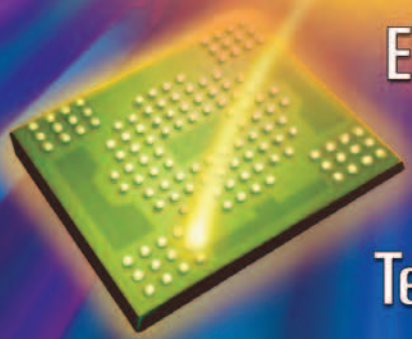
Memory Test

Testing Mobile Memories









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PXI/VXI Buyers Guide

www.evaluationengineering.com

Testing Mobile Memories

by Kurt Gusinow, Agilent Technologies

It's a phone. No, it's a camera...a computer...a TV. Whatever you call it, it's a huge test challenge for memory manufacturers.

As we expect our mobile phones to play MP3s, take still pictures, provide PDA functionality, and stream video, the required amount and types of memory increase. This convergence in the mobile communications market combined with ever-shrinking form factors drives manufacturers to consider different packaging solutions for mobile memories.

One solution is to package the various types of memory required for these devices in a single multichip package (MCP). This helps manufacturers offer new multifunction devices without increasing the overall size of the end product. With the enhanced functionality that the MCPs enable come new test challenges for memory manufacturers.

Divergent Requirements

In 1990, I was sure to impress those around me whenever I pulled out my mobile phone. Immediately everybody knew that I was too important to ever be out of touch.

Now the world has changed. My stepfather uses his mobile phone to watch the Kings basketball team while he takes his grandson for a walk. Going outside no longer stops my nephew from playing his games. And my boss never is really in a meeting but rather in two or three since he always is either TXTing or e-mailing somebody with his phone.

With mobile phones, one thing is certain: They are no longer just for talking. As they become our means of staying connected to each other and the Internet, trade-offs must be made among functionality, battery life, price, and size.

Many of these trade-offs relate directly to the types of memory chosen for the phone. My first mobile phone had a small amount of NOR flash, maybe 8 Mb, for storing the program that ran the phone. It also had an even smaller amount of low-power SRAM, maybe 1 Mb, that served as working memory because the program time of flash is too long.

This combination worked well, and the natural bit growth of the NOR and SRAM met the growing requirements for phones until the inclusion of large color screens, high pixel-count cameras, and MP3 player capability drove the need for the ultra-high densities of NAND flash. Now the applications processors that allow phones to perform as PDAs, portable game players, and televisions require NAND flash to store the complex programs and mobile SDRAM performance to provide the user with the best possible experience.

So how do you increase the memory in a mobile phone from 8 Mb to more than 1 Gb, go from two types of memory to four, and fit all of this memory in less space? The answer: memory must grow up.

3-D Package Technology

There are several 3-D packaging technologies, each with a unique value proposition of size, cost, and flexibility. At one end is the system-in-package (SIP) technology in which the memory is packaged on top of the processor, and there may be several passive components in the same package. This results in the smallest form factor, possibly even a one-chip phone.

However, one bad die in the stack means the whole SIP will fail. This yield loss might be acceptable for memories that cost a few dollars, but processors cost about $20, making this an expensive alternative. Since the stack must be designed together, any change to any of the dice could change the stack, requiring longer lead times and limiting flexibility.

A more recent technology is package-on-package (POP). This technology

provides the greatest flexibility, allowing phone manufacturers to choose the memory stack and the memory suppliers during production instead of during the initial design phase. Dealing with separately packaged dice comes at a price: The stacks are physically higher, multiple individual packages cost more than a single package, and POP technology comes at a premium because the IP is patented.

MCPs offer a good compromise: small footprint, low cost, and reasonable flexibility. Like a SIP, an MCP encapsulates multiple dice in a single package. Because the MCP only includes memories, the design of the processor is independent of the memory specifics, which is important given the fast turns and short life cycles of DRAM and NAND.

The resulting low-profile, low-cost package has become the standard for mobile phones with nearly all of them having at least one MCP. While SIP, POP, and other exotic technologies such as package-in-package (PIP) are making some inroads in the 3-D packaging market, MCPs are expected to continue to dominate for the next five years.

Segregated Memory Buses

The first MCPs going into mobile phones contained a NOR flash and an SRAM. Because the addressing protocols for the two memories are similar and because they both provided memory to the baseband processor, their data and address pins were shared. The result was a flash memory with a few extra control pins for the SRAM.

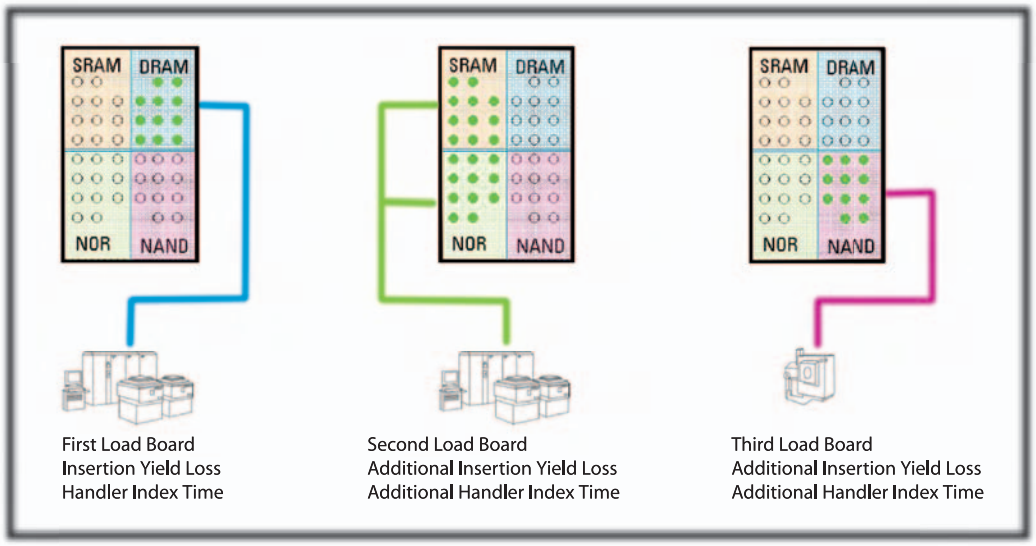

Figure 1. Multiple Insertion Technique

But as phones are required to do more than just transmit voice, phone manufacturers are responding by adding an applications processor. While a fundamental requirement for the baseband processor is to minimize power consumption, the applications processor focuses on performance. As a consequence, the SDRAM resides on a higher performance bus. Finally, the NAND flash, which provides nonvolatile high-density data storage, may reside on yet another bus because of its lower performance and significantly different protocol.

A stack of these memories might reside on three buses: a NOR/SRAM, a higher performance SDRAM, and a NAND. This is no longer a simple memory device but may have as many as 133 signal pins including 66 bidirectional pins.

Constraints Maximize Cost

A standard memory tester customarily reduces cost by testing as many devices as possible in parallel. The newest testers accommodate up to 256 sites in parallel. This parallelism is an absolute requirement because larger memory densities increase test time and cost.

Indeed, DRAM testers are designed to be massively parallel with a fixed number of timing functions, less than 64, fanned out across all of the devices. This works quite well for standard memories with less than 64 signal pins but is not sufficient for an MCP with 133 pins.

The current solution is to test the MCPs on multiple testers (**Figure 1**). The SDRAM is tested on a DRAM tester. Then, the MCP is transferred to another tester with another load board that connects the NOR/SRAM to be tested. Finally, the MCP is moved to a third tester, possibly a flash tester, where yet a third load board connects the NAND to be tested.

The three insertions increase the total test time of the MCP and overall test-floor complexity, both of which result in a higher cost of test. Additionally, the process triples the yield-loss due to parts that are damaged through handling.

A possible solution is to use a tester that can accommodate devices with more than 64 pins. All of the pins can be connected and all of the devices tested in one test insertion. This solves the multiple insertion problem but results in a low utilization of tester resources: the SRAM and DRAM finish testing much more quickly than the NOR and NAND.

MCPs offer a good compromise: small footprint, low cost, and reasonable flexibility.

To reduce the pin-count, some MCPs have common pins among some of the dice. This limits the capability of the dice to be operated or tested in parallel. Additionally, memory manufacturers often will want to run some tests sequentially through the stack to prevent or measure die-to-die interaction such as crosstalk and ground bounce.

If the memories must be tested sequentially, then the tester resources connected to the memories not currently under test sit idle. This could be as much as two-thirds of the tester being idle on average. In both of these scenarios, you are paying for resources that may sit idle most of the time.

Flexibility Minimizes Cost

To maximize tester resource use and minimize the amount of tester resources that must be purchased, tester functions must be rerouted to pins that are being tested at a specific point in the flow. This reroutable interface technique tests the MCP in a single insertion and at a high parallelism while ensuring the highest utilization. Yet, as with many ideas, complications lie in the details.

The first obstacle is the sheer number of signals to be rerouted. If 40 signals per device must be reroutable to one of four device pins, a minimum of 120 relays per site are required. If 64 devices are tested in parallel, 7,680 relays are required. Not only does this take up a tremendous amount of space and burn a great deal of power, but, more importantly, it also creates a significant reliability risk.

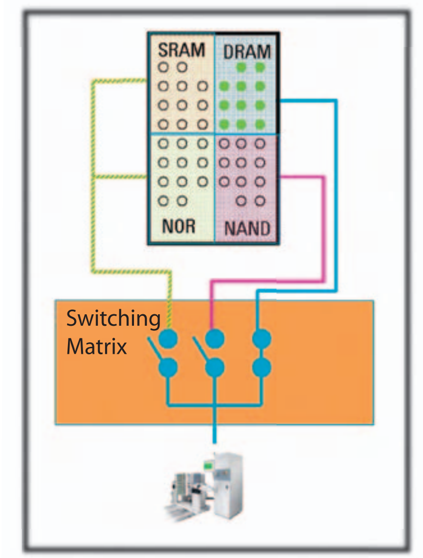

Figure 2. Single Insertion, High-Parallelism, High Resource Utilization

Discrete FET switches help with the board space but have their own issues. Their capacitance and trace-length stubs can impact the frequency performance to the DUT. If MCPs only had flash, the performance degradation might be acceptable, but mobile SDRAMs are already running at 133 MHz, and mobile games surely will drive even higher performance. High-performance FETs are available, but these are quite sensitive to ESD and, as a result, can be unreliable.

The use of a high-performance ASIC can help resolve many of these issues. Trace-length stubs are minimized, and tremendous switching densities can be achieved. The long lead times and cost of the ASIC require that this switching matrix be device independent. It is too costly to redesign this matrix for every device that is to be tested.

An additional interface layer must be provided. This creates additional challenges because a very high-density, highly reliable, and high performing interconnect must be used. Also, every tester channel must have the same functionality. Otherwise, the routing from the switching matrix to the device pin will be extended, degrading performance and adding channel capacitance.

Having all identical channels offers the benefit of reusing the device-specific interface or socket board. Because MCPs are designed for a specific mobile appliance, there is no consistency in pinouts for a given package.

While JEDEC is attempting to mitigate this by setting standards, ever in-

Performance Comes in a Small Package

Realizing that 16,384 relays (4 relays × 4,096 channels) could not be a reliable switching matrix, Agilent developed the Kiowa, a high-performance ASIC that provides the switching mechanism for four tester channels. The key design criteria for the ASIC revolved around performance, size, and reliability.

To achieve the required performance, the switching matrix cannot increase the signal path capacitance substantially. Increased capacitance will slow down the rise times of high-performance memories, and many lower performance mobile memories cannot drive a highly capacitive line.

To this end, line capacitance was minimized by simplifying the signal path as much as possible and using less capacitive gates. The routing was implemented to minimize the stub length for each switch path since each stub increases the capacitance for the line. Finally, each channel is isolated from the other three channels to minimize any crosstalk between channels.

To accommodate 1,024 ASICs per test head, a 100-pin chip scale package (CSP) was chosen. The high-speed serial bus minimizes the number of traces that must be run to each ASIC, resulting in a less complex, smaller board.

Due to the static that can build up as parts are inserted into a socket, ESD had to be taken into account. In addition to diode-clamping the ground and supply pins, each tester channel is connected to a low equivalent series resistance (ESR), low-inductance 100-nF capacitor. The slight decrease in performance from the increased line capacitance is well justified by the increased reliability of the switch.

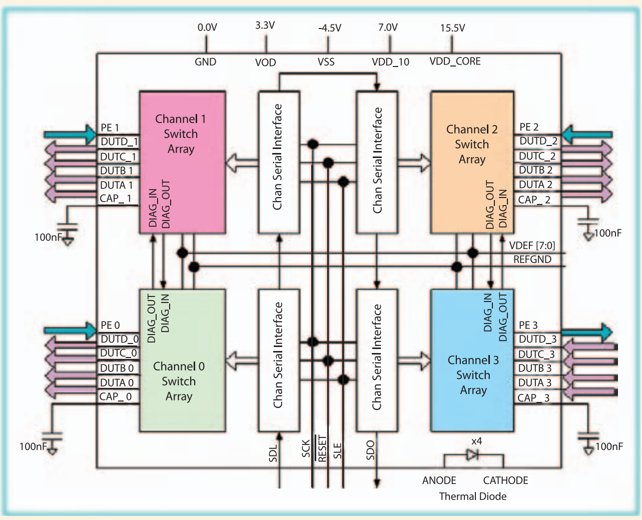

Figure 3. The Kiowa Switching ASIC

		High Pin-Count Tester	Memory Tester	All I/O + Switching Matrix
8 Dice MCP (133 pins)	# of Insertions	1	3	1
	# of Load Boards (~$100k)	1	3	1
	Parallelism (4,096 pins/head)	32	64	64
	Total Test Time	100	120	100
	Test Time/Device	3.13	1.88	1.56
	Cost/Socket (no tester)	$3,125	$4,688	$1,563
	Tester Resource Utilization	33%	95%	99%
4 Dice MCP (80 pins)	# of Insertions	1	2	1
	# of Load Boards (~$100k)	1	2	1
	Parallelism (4,096 pins/head)	50	64	128
	Total Test Time	100	120	100
	Test Time/Device	2.00	1.88	0.78
	Cost/Socket (no tester)	$2,000	$3,125	$781
	Tester Resource Utilization	50%	95%	99%

Table 1. Cost of Test Comparison of MCP Test Solutions

creasing time-to-market pressure drives vendors to reuse package designs for various stacks. For example, pin M5 may be an I/O for a NAND flash for one MCP, and it may be an address pin for a NOR flash on another MCP. The tester must deliver a clock, address, or I/O signal to any pin.

If the tester manufacturer has reduced cost by optimizing channels to deliver specific functionality to a channel, the correct type of tester channel must be routed to the pin for only that device. Each MCP will require its own interface board. This cost is further exacerbated as device life cycles continue to decrease.

Reducing the Cost of Testing MCPs

A switching network in conjunction with an all-I/O tester increases tester resource use when testing MCPs (**Figure 2**). The higher resource utilization allows for higher parallelism and shorter test times. The switching network also can test complex MCPs in one insertion, saving multiple load boards that would have to be designed and built for each new MCP.

Because of the high parallelism, relays are not an option. Meanwhile, the performance of mobile SDRAMs forces the switching network to be in a high-performance ASIC. The long design times and high costs of an ASIC require that this solution be implemented independently of any device-specific hardware, such as load boards. This also allows the reuse of load boards for multiple devices.

Technology pundits everywhere are trying to predict what applications will go into future cell phones. They might all be wrong. But one thing is certain: We will want more and more from our phones while expecting them to become smaller and smaller. These increased densities will continue to drive the higher level of integration that MCPs provide.

As the stacks grow higher, providing economic testing becomes increasingly difficult. As shown in **Table 1**, a switching matrix can reduce the cost of test by up to 75%, helping to reduce the price of 3G phones.

About the Author

Kurt Gusinow is the market development manager for memory test at Agilent Semiconductor Test Systems. He has spent the last 15 years in the ATE industry after graduating from the University of California with a B.S.C.E. Agilent Technologies, e-mail: kurt_gusinow@agilent.com

EE

Reprinted from *EE-Evaluation Engineering*, September 2005

Exhibit K

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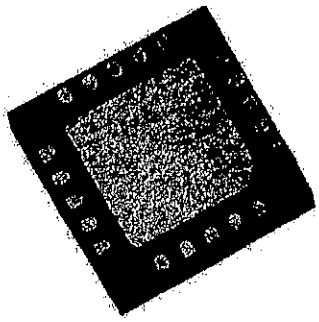
Exhibit L

HRF-SW1020

Honeywell

SP4T Absorptive RF Switch DC To 2.5 GHz Operation

The Honeywell HRF-SW1020 is a high performance single pole four throw (SP4T) absorptive RF switch that is ideal for use in wireless basestation and handset applications that require minimum power and minimum insertion loss.



The HRF-SW1020 is manufactured with Honeywell's patented Silicon On Insulator (SOI) CMOS technology, which provides the performance of GaAs with the economy and integration capabilities of conventional CMOS technology. These switches are DC coupled to improve lower operating frequency, frequency response and reduce the number of DC bias points required.

FEATURES

- Typical High Isolation Of > 40 dB @ 2 GHz
- Typical Low Insertion Loss Of 1.7dB @ 1 GHz
- Integrated CMOS Control Logic
- DC-coupled, bi-directional RF Path
- Single Positive Supply Voltage
- Ultra Small VQFN Packaging
- Impedance matched for 50 Ohm systems

RF ELECTRICAL SPECIFICATIONS @ + 25°C

Results @ V_{DD} = 5.0 +/- 10%, V_{SS} = 0 unless otherwise stated, Z_0 = 50 Ohms
Contact Honeywell for relative performance at other supply configurations

Parameter	Test Conditions	Frequency	Minimum	Typical	Maximum	Units
Insertion Loss		1.0 GHz 2.0 GHz 2.5 GHz		1.6 1.7 1.8	1.9 2.2 2.3	dB dB dB
Isolation		1.0 GHz 2.0 GHz 2.5 GHz	45 33 30	54 41 39		dB dB dB
Return Loss			-15	-20		dB
Input P1dB	V_{SS}= Gnd V_{SS} = -5V	1.0 GHz 1.0 GHz		17 27		dBm dBm
Input IP3	Two-Tone Inputs, up to + 5 dBm V_{SS} = Gnd V_{SS} = -5V	2.0 GHz 2.0 GHz		35 36		dBm dBm
Trise, Tfall Ton, Toff	10% To 90% 50% Cntl To 90% / 10% RF			10 20		ns ns

HRF-SW1020

DC ELECTRICAL SPECIFICATIONS @ + 25°C

Parameter	Minimum	Typical	Maximum	Units
V_{DD}	3.3[1]	5.0	5.5	V
V_{SS}	-5.0			V
I_{DD}		<5	35	uA
CMOS Logic Level (0)	0		0.8	V
CMOS Logic Level (1)	V_{DD} – 0.8		V_{DD}	V
Input Leakage Current			10	uA

Note 1 - Performance curves are for VDD = +5.0 +/- 10%

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Absolute Maximum	Units
V_{DD}	+6.0	V
V_{SS}	-5.5	V
Vin Digital Logic 0	-0.6	V
Vin Digital Logic 1	Vdd + 0.6	V
Input Power	> 35	dBm
ESD Voltage[2]	400	V
Moisture Sensitivity Level	Level 3 @ 240°C	
Solder Reflow Temperature	250	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +125	°C

Note 1 - Operation of this device beyond any of these parameters may cause permanent damage.
Note 2 - Although the HRF-SW1020 contains ESD protection circuitry on all digital inputs, precautions should be taken to ensure that the Absolute Maximum Ratings are not exceeded.

Latch-Up: Unlike conventional CMOS digital attenuators, Honeywell's HRF-SW1020 is immune to latch-up..

TRUTH TABLE

C1	C0	RFOUTPUT1	RFOUTPUT2	RFOUTPUT3	RFOUTPUT4
0	0	RFINPUT			
0	1		RFINPUT		
1	0			RFINPUT	
1	1				RFINPUT

"0" = CMOS Low, "1" = CMOS High

PIN CONFIGURATIONS

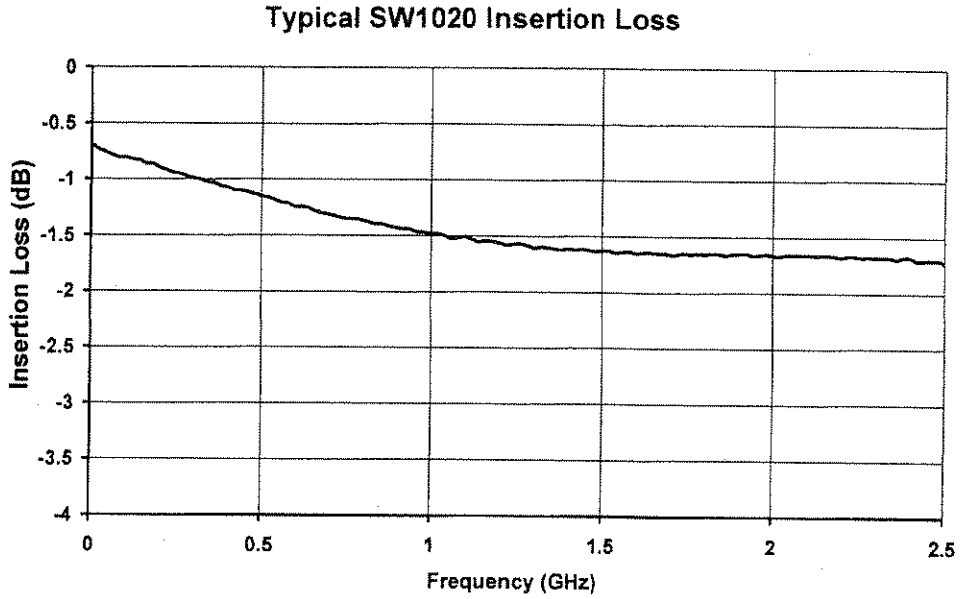
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GROUND	6	RFOUTPUT3	11	C1	16	GROUND
2	RFOUTPUT4	7	GROUND	12	C0	17	GROUND
3	GROUND	8	GROUND	13	GROUND	18	RFINPUT
4	VDD	9	GROUND	14	RFOUTPUT1	19	GROUND
5	GROUND	10	RFOUTPUT2	15	GROUND	20	VSS

Note: Bottom ground plate must be grounded for proper RF performance.

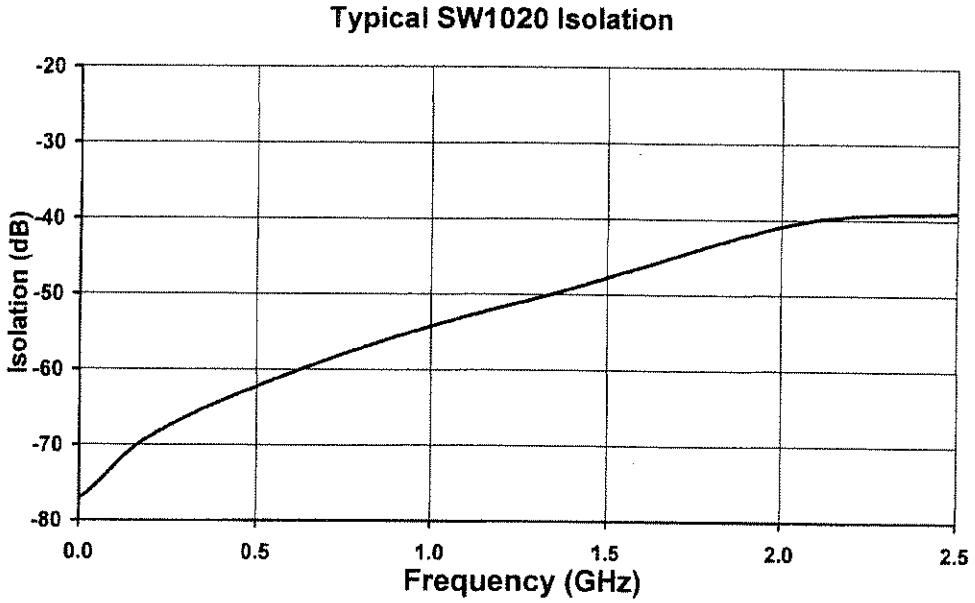
HRF-SW1020

PERFORMANCE CURVES

Insertion Loss

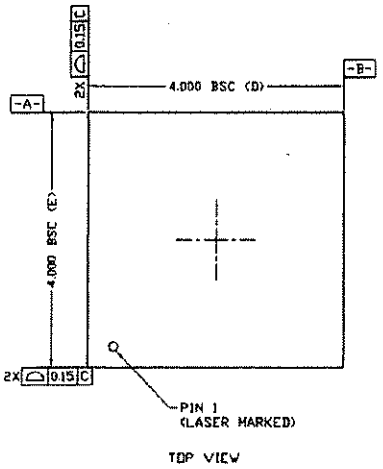


Isolation

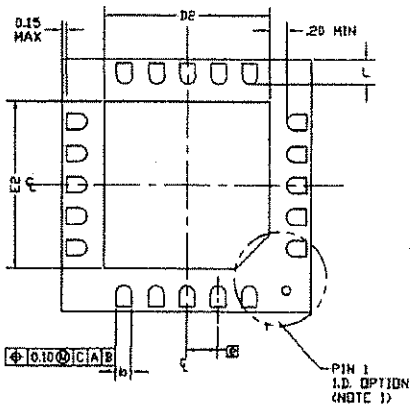


HRF-SW1020

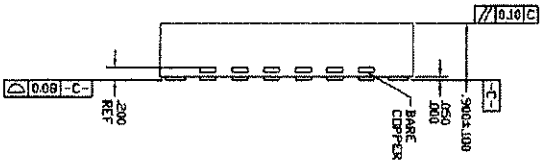
PACKAGE OUTLINE DRAWING



TOP VIEW



BOTTOM VIEW



SYMBOL	MIN	NOM	MAX
e		0.50 BSC	
b	0.18	0.25	0.30
E2	2.55	2.65	2.75
D2	2.55	2.65	2.75
L	0.35	0.40	0.45
INTERNAL FEATURE	FUSE LEAD		

Notes

1. Pin 1 identifier can be a combination or a dot and/or chamfer.
2. Dimensions are in millimeters.

LEAD FINISH

The package leads are Nickel Palladium Gold (NiPdAu). The configuration being manufactured and delivered today is lead-free RoHS compliant. Compliant packages have half-etch leadframes and have date codes of 0300 or greater.

LEAD FREE QFN SURFACE MOUNT APPLICATION

Please see Application Note AN310 for assembly process recommendations. Application Notes can be found at our website: www.honeywell.com/microwave

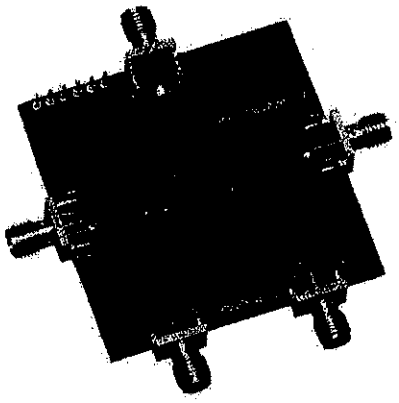
CIRCUIT APPLICATION INFORMATION

These attenuators require a DC reference to ground. They may not operate properly when AC coupled on both the RF input and output without a DC ground reference provided as part of the circuit. See Application Note AN311.

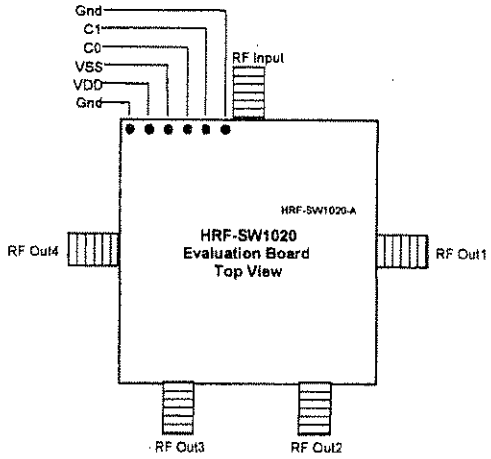
HRF-SW1020

EVALUATION CIRCUIT BOARD

Honeywell's evaluation board provides an easy to use method of evaluating the RF performance of our switch. Simply connect power; DC and RF signals to be measuring switch performance in less than 10 minutes.



HRF-SW1020 Evaluation Board



EVALUATION CIRCUIT BOARD LAYOUT DESIGN DETAILS

Item	Description
PCB	Impedance Matched Multi-Layer FR4
Switch	HRF-SW1020 RF Switch
Chip Capacitor	Panasonic Model ECU-E1C103KBQ Capacitor, .01uf 0402 10% 16V
RF Connector	Johnson Connectors Model 142-0701-801 SMA RF Coaxial Connector
DC Pin	Mil-Max Model 800-10-064-10-001 Header Pins

ORDERING INFORMATION

Ordering Number	Delivery Method	Quantity Per Shipment
HRF-SW1020-AU-TR	Tape & Reel	2500 Units per Reel
HRF-SW1020-AU-T	Tape	< 2500
HRF-SW1020- E	Evaluation Board	One Board Per Box

FIND OUT MORE

For more information on Honeywell's Microwave Products visit us online at **www.honeywell.com/microwave** or contact us at 800-323-8295 (763-954-2474 internationally).

Honeywell
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Plymouth, MN 55441
Tel: 800-323-8295
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Form #1020W
January 2007

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Exhibit M

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